Digital IP Core

RISC_CPU_5X

“RISC_CPU_5X”

SERMA PRODUCTIVITY ENGINEERING

General Description

The digital IP Core “RISC_CPU_5X” is a PIC16C5X compliant, modular designed microcontroller core, which is provided for insertion to ASICs with controller functions. This Core is useable as basic module for customer DSP functionality.

Features:

- Compatible Implementation of PIC16C5X instruction set
- Every instruction cycle use one clock cycle (cp. four clock cycles in original PIC16C5X)
- Execution of first instruction in first clock directly after reset
- Modular structure for add-ons and customizations
- Totally digital design
- Technologically independent

Ratings, Parameters and Conditions

Description:
VHDL

Parameters:
12 bit data bus, 11 bit address bus, 3 Ports with 8 bit bidirectional I/O, 72 byte GPR

Frequency range:
35MHz (0,35um LPower XFAB-Technology, XH035-Process, 2LM)
90MHz (0,18um LPower XFAB-Technology, XC018-Process)

Dimension / Range (approximately):
0,142 mm^2 (0,35um LPower XFAB-Technology, XH035-Process, 3LM); 0,244 mm^2 (2LM).
0,023 mm^2 (0,18um LPower XFAB-Technology, XC018-Process).
1k (2,5k with internal GPR) Equivalent Gates

Number of ports: 7 (49 bit)

IO-Description

Interface	I/O	Function Comment
CLK_I	Input	System clock
RESET_NI	Input	Reset low active
PADDR_O	Output	11 bit Address for Program Memeory
PDATA_I	Input	12 bit Data from Program Memory
PORT_A_B	InOut	8 bit Bidirectional I/O-Port
PORT_B_B	InOut	8 bit Bidirectional I/O-Port
PORT_C_B	InOut	8 bit Bidirectional I/O-Port

Symbol / external schematic