Analog IP Cell

Relaxation Oscillator

RelaxOSC XC10LV

SERMA PRODUCTIVITY ENGINEERING

General Description

The analogue IP cell RelaxOSC XC10LV is a relaxation oscillator optimized for low supply voltage operation and low power consumption. Because of its supply voltage range it can be used in single battery cell operated designs.
The cell is designed for a nominal operation frequency of 1.66MHz and can be trimmed to this value using a 4Bit wide trim input. In typical application, Poly-Si fuse cells are used a non-volatile memory holding the trim information.
An enable input is implemented to power down the cell is the clock is not needed. Else two non-overlapping clock signals are generated with a very short start up time.

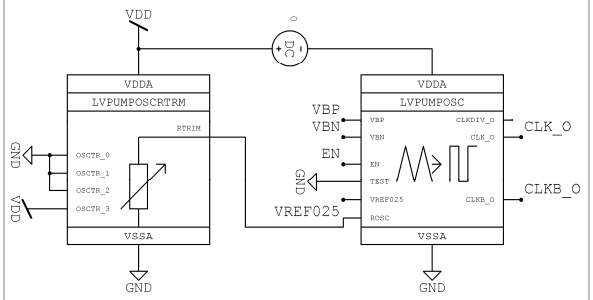
Ratings, Parameters and Conditions

Parameter / Condition	Symbol	Min	Typ.	Max	Unit	Comment
Electrical Parameters:						
Supply Voltage	V_{dd}	1.3	1.55	1.6	V	
Active Supply Current	I_{dd}	6	12	22	µA	depending on output frequency
Inactive Supply Current	I_{ddidle}			25	nA	
Frequency Trimming Range typical case	$F_{CLKTRIM}$	1	1.66	2.5	MHz	
Frequency Accuracy trimmed over Voltage and Temperature	F_{CLKTM}	1.62	1.66	1.73	MHz	trimmed to 1.66MHz, typical case
Power Up Time	T_{SU}			100	µs	
Clock Duty Cycle	DC_{CLK}	45	48	60	%	
Absolute Maximum Ratings:						
Operating Temperature	T_{range}	-40		140	℃	
Supply Voltage	V_{dd}	-0.3		6	V	
Input Voltage	V_{in}	-0.3		V_{dd}+0.7		
Output Voltage	V_{out}	-0.3		V_{dd}+0.7		
Operating Conditions:						
Ambient Temperature	T_{amb}	-20	27	80	℃	

IO-Description

Interface	I/O	Function	Comment
VSSA	input	Supply	
VDDA	Input	Supply	
OSCTR_0-3	Inputs	Trim Inputs	
VREF025	Input	Reference Voltage Input	nom. 150mV
EN	Input	Enable Sig.	
VBN	Input	N Bias Voltage	
VBP	Input	P Bias Voltage	
TEST	Input	Test enable	
CLKDIV_O	Output	FCLK/1024	only active when Test=H
CLK_O	Output	Clock Output	
CLKB_O	Output	inverted Clock Output	

Block schematic, ext. component diagram



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