Analog IP Cell

Power On Reset Circuit

POR XC10LV

SERMA PRODUCTIVITY ENGINEERING

General Description

In mixed signal ASIC designs a reliable start up of the digital core has to be ensured. A power on reset circuit is normally used for this purpose.
The analogue IP cell POR XC10LV is a low power, low voltage optimized cell intended to be used in single battery cell operated mixed signal ASIC applications. The cell has no static power consumption after power up, only unavoidable leakage currents remain. Both a high-level active and low-level active reset signal is available.

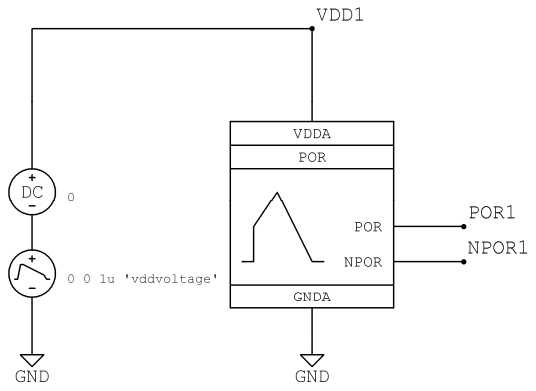
Ratings, Parameters and Conditions

Parameter / Condition	Symbol	Min	Typ.	Max	Unit	Comment
Electrical Parameters:						
Supply Voltage	V_{dd}	1.3	1..5	1.6	V	
Active Supply Current before POR	I_{ddBSU}			1	µA	
Active Supply Current after POR	I_{ddASU}			50	nA	
POR delay	T_{POR}	25	400	3000	us	
Power Up Threshold	V_{POR}		1.2		V	
Absolute Maximum Ratings:						
Operating Temperature	T_{range}	-40		140	℃	
Supply Voltage	V_{dd}	-0.3		6	V	
Input Voltage	V_{in}	-0.3		V_{dd}+0.7		
Output Voltage	V_{out}	-0.3		V_{dd}+0.7		
Operating Conditions:						
Ambient Temperature	T_{amb}	-20	27	80	℃	

IO-Description

Interface	I/O	Function	Comment
GNDA	input	Supply	
VDDA	Input	Supply	
POR	Output	Power On Reset Signal	low after POR
NPOR	Output	Inverted Power On Reset Signal	high after POR

Block schematic, ext. component diagram



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