Digital IP Core

pWire Master

SERMA PRODUCTIVITY ENGINEERING

General Description

The digital IP Core “pwire_master” is a master protocol handler for pWire interfaces and provides a synchronous interface to pWire slaves and Dallas Semiconductor 1-Wire®, iButton® devices.

It is customizable with generic parameters for:

- speed mode
- length of transfer cycle
- period of system clock

Ratings, Parameters and Conditions

Description:
VHDL, EDIF

Generic Parameters:

SPEED_MODE_G	Speed mode: 0 = regular speed, 1 = overdrive speed
D_WIDTH_G	Length of transfer cycle, Width of data port “din_i” and “dout_o”
CLK_PERIOD_G	Real clock period in nanoseconds

Frequency range:
2 – 80 MHz (±30%), at regular speed
8 – 80 MHz (±20%), at overdrive speed

Dimension / Area consumption (approximately):
0,18 mm^2 (0,6um LPower Tech. 2LM, regular speed, 8-Bit Data Width, 60 MHz),
0,09 mm^2 (0,6um LPower Tech. 3LM, overdrive speed, 8-Bit Data Width, 8 MHz).

Number of ports: 8 + D_WIDTH_G*2

IO-Description

Interface	I/O	Function Comment
clk	Input	System clock
rstn	Input	Reset (asynchrony, Lo-activ)
opcode_i	Input	Operation (00 = NOP, 01 = Send Reset Slot, 10 = Send Data, 11 = Receive Data
din_i	Input	Send Data Port
dout_o	Output	Recive Data Port
dout_en_o	Output	Data of Recive Data Port is current
ready_o	Output	Ready for new data transfer
presence_o	Output	Request of Reset Slot (1 = presence pulse received)
one_wire_io	BiDi	One Wire Port (Open Drain)

Symbol / external schematic