Digital IP Core

I²C Master

SERMA PRODUCTIVITY ENGINEERING

General Description

The digital IP Core “i2c_master” is a fully compliant I²C-Multi-Master-Interface.

Features:

- Programmable I²C clock frequency
- Transmission speeds from normal (100kbps) to high speed (3,5 Mbps)
- Start, Stop, Repeated Start and Acknowledge generation
- Collision detection and arbitration

Ratings, Parameters and Conditions

Description:
VHDL

Parameters:
8 bit of data per I²C Cycle

Preload SCL stretching register with: $\text{Preload} = \frac{CLK_{frequency}}{4 \cdot SCL_{frequency}} [HEX]$; $\text{Preload}_{default}$ = 0xFFFF

Frequency range:
1 – 70 MHz

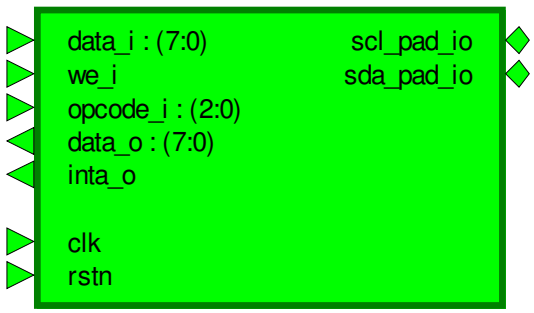
Area consumption (approximately):
0,6 mm^2 (0,6um, 2LM)
0,09 mm^2 (0,35um, 3LM)

Number of ports: 25

IO-Description

Interface	I/O	Function Comment
clk	Input	System clock
rstn	Input	Reset (asynchrony, Lo-activ)
opcode_i	Input	Operation
data_i	Input	Data input port
we_i		Write Enable
data_o	Output	Data output port
inta_o	Output	Interrupt signal
scl_pad_io	BiDi	I²C-SCL-Wire
sda_pad_io	BiDi	I²C-SDA-Wire

Symbol / external schematic



i2c_master