Analog IP Cell

Clock multiplier - quadruple

XDH10

General Description

This cell is especially designed for low power applications. It employs a simple clock doubler architecture to save power. The output clock is four times higher than the input clock but duty cycle is not constant over process and temperature variation. The digital circuit that will be supported by this circuit has to be able to withstand this variation. This block was designed to perform a very dedicated functionality. For higher accuracy requirements refer to the PE PLL IP cells.

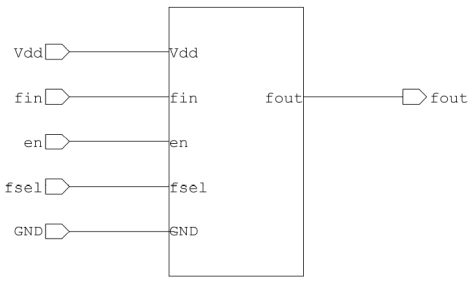
Ratings, Parameters and Conditions

Parameter / Condition	Symbol	Min	Typ.	Max	Unit	Comment
Electrical Parameters:						
Supply Voltage	V_{dd}	4,5	5,0	5,5	V	
Supply Current	I_{dd}	70	110	187	µA	
Input Frequency	F_{IN}		2		MHz	
Output Frequency	F_{out}		8		MHz	
settling Time	T_{stl}		<2		µs	
Low Time	t_{low}	11		158	ns	f=8 MHz
High Time	t_{high}	30		105	ns	f=8 MHz
FANOUT			2			
Absolute Maximum Ratings:						
Operating Temperature	T_{range}	-40		125	℃	
Supply Voltage	V_{dd}	-0.3		7	V	
Input Voltage	V_{in}	-0.3		V_{dd}+0.7		
Output Voltage	V_{out}	-0.3		V_{dd}+0.7		

IO-Description

Interface	I/O	Function	Comment
VDD	Input	Supply	
GND	Input	Supply	
FIN	Input	Clock Input	2MHz
EN	Input	Enable	
FSEL	Input	Multiplexer	FOUT=FIN
FOUT	Output	Frequency Output	8MHz

Symbol / external schematic



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