LEON3

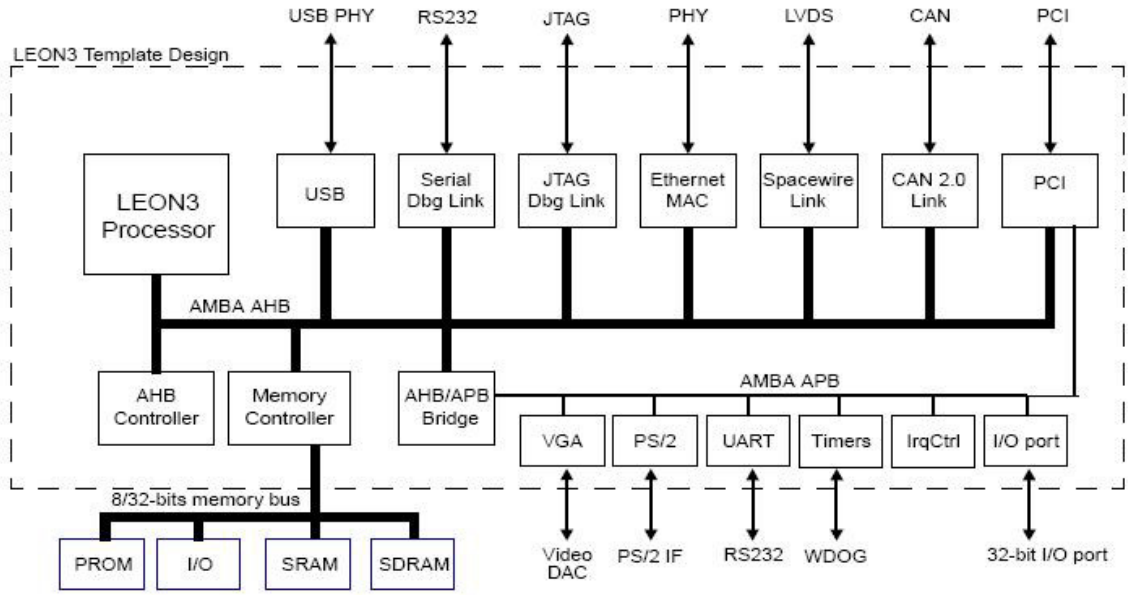
32bit RISC CPU

SERMA PRODUCTIVITY ENGINEERING

Features

- fully 32 bit SPARC V8 compatible instruction set
- 7-stage pipeline
- highly configurable (branch prediction, cache-size, memory interface, FPU, MMU, etc.)
- several peripheral units available (PCI, VGA, UART, SPI, I²C, Ethernet, etc.)
- small core area (~ .6 mm² on 180 nm)
- 2-32 register windows for less spill/fill operations and efficienct function calls
- Rad-Hard on request

Functional Block Diagram



General Description

The LEON3 is a 32-bit RISC Microprocessor with fully compatible SPARC V8 instruction set. It is highly configurable and comes along with several peripheral options. Productivity Engineering offers to integrate the core into a SOC, combined with additional digital and analog functions. Since the processor can be fully simulated including the application programm, PE can help customers to choose the right configuration to satisfy all customer needs. A complete development environment is available. Evaluation in an FPGA is possible. This minimizes the design-risk and allows software-development during IC-manufacturing, resulting in a shorter time-to-market. As a plus, the core is available under GNU GPL licence, reducing system cost.