Analog IP Cell

RFID HF Frontend

HF-FE XH035

SERMA PRODUCTIVITY ENGINEERING

General Description

The HF-FE IP Cell is an RFID Front-end for passive 13,56MHz Tag ICs.
In HF applications power is coupled contactless to the front-end (magnetic coupling).
This IP Cell implements a rectifier for operation voltage and a regulator for the digital supply voltage, a demodulator with reset and a modulator for communication from Reader to Tag and from Tag to Reader. The reset signal can also be used to disable the demodulator. Furthermore the front-end consist of a clock extractor and a power on reset (POR).
A bias source provides currents and voltages for the analog and digital blocks.
This IP Cell is designed in accordance with the **ISO15693** (ASK modulation from reader to tag and load modulation from tag to reader). It is designed to operate with PE's ISO15693 digital protocol engine IP cell and can be used for smart RFID applications that employ sensor and communication technology, e.g. in medical applications or logistics control.
The IP cell has a cell size of <0,4mm² in 0,35um CMOS technology.

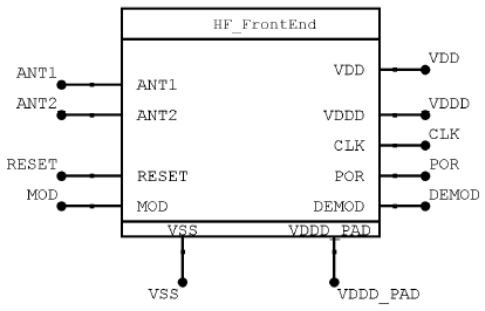
Typical Ratings, Parameters and Condition

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Operation temperature	T_{op}	-40	27	80	℃	
Frequency	f_{CLK}		13.560		MHz	
Antenna voltage	V_{ANT}			5,5	V	
Rectified voltage	V_{DD}			4,7	V	
Digital supply voltage	V_{DDD}	1,8	2	2,2	V	
Ripple digital supply voltage	$V_{DDDripple}$	20		300	mV	
Current consumption	I_{DD}	15	20	30	uA	
Active current	I_{DDD}	30			uA	
Power on Reset	t_{POR}	45			us	
Load modulation frequency	f_{Mod}		423,75		kHz	ISO15693 (1 subcarrier)
	f_{Mod}		484,28		kHz	ISO15693 (2 subcarrier)
ASK modulation	t_{Demod}	6		13,94	us	ISO15693

IO-Description

Interface	I/O	Function	Comment
ANT1	In/Out	Antenna	
ANT2	In/Out	Antenna	
VDDD_PAD	In/Out	Supply	digital pads supply
VDDD	Out	Supply	digital supply
VDD	In/Out	Supply	Rectified voltage
VSS	In/Out	Supply	Ground
MOD	In	Digital	load modulation
RESET	In	Digital	demod reset
CLK	Out	Digital	Extracted clock
POR	Out	Digital	Power on reset
DEMOD	Out	Digital	Demod signal

Symbol / external schematic



Dieses Projekt wird mit Mitteln des Europäischen Sozialfonds (ESF) gefördert. Es erzeugt einen gemeinschaftlichen Mehrwert „Investition in Ihre Zukunft".