Analog IP Cell

Comparator for ADC

XH018

SERMA PRODUCTIVITY ENGINEERING

General Description

This cell is a fast clocking comparator with offset cancelation. It uses 2 clocks for offset canceling and latching. The input signal is coupled via capacitors. It accepts rail to rail or higher signal levels. Only the difference is being used.

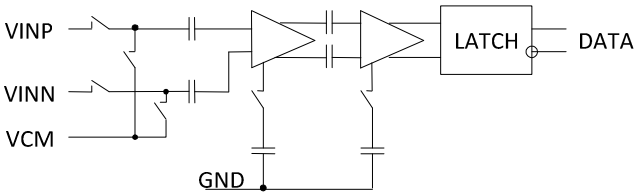

Figure 1: Functional Schematic

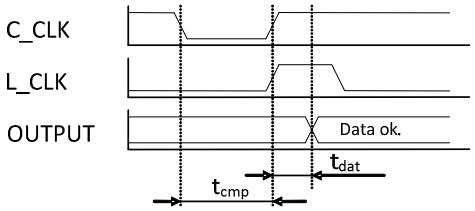

Figure 2: Timing Diagram

Ratings, Parameters and Conditions

Absolute Maximum Ratings						
Parameter / Condition	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Comment**
Operating Temperature	T_{OP}	-40		120	℃	
Supply Voltage	V_{DD}	-0.3		3.6	V	
Input Voltage	V_{IN}	-0.3		V_{DD}+0.7	V	
Output Voltage	V_{OUT}	-0.3		V_{DD}+0.7	V	

Electrical Parameters						
Parameter / Condition	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Comment**
Operating Temperature	T_{OP}	-40		85	℃	
Supply Voltage	V_{DD}	3.0	3.3	3.6	V	
Current Consumption	I_{DD}		100		µA	10µA BIAS current
Comparator time	t_{cmp}	8			ns	
Data delay	T_{dat}			4	ns	min L_CLK high time
Input Voltage	V_{IN}	0		V_{DD}	V	
Offset Voltage	V_{offs}			±300	µV	

Interface and Symbol

Nr.	Name	I/O	Bezeichnung
1	VCM	I	Common voltage
2	VBN	I	BIAS voltage
3	INNCMP	I	Input positive
4	INPCMP	I	Input negative
5	C_CLK	I	Comparator clock
6	L_CLK	I	Latch clock
7	RESET	I	Reset high-active
8	CLK1o	O	Comparator clock delayed
9	Q	O	Output high-active
10	QN	O	Output low-active
11	VCC	P	Supply voltage
12	VSS	P	Ground