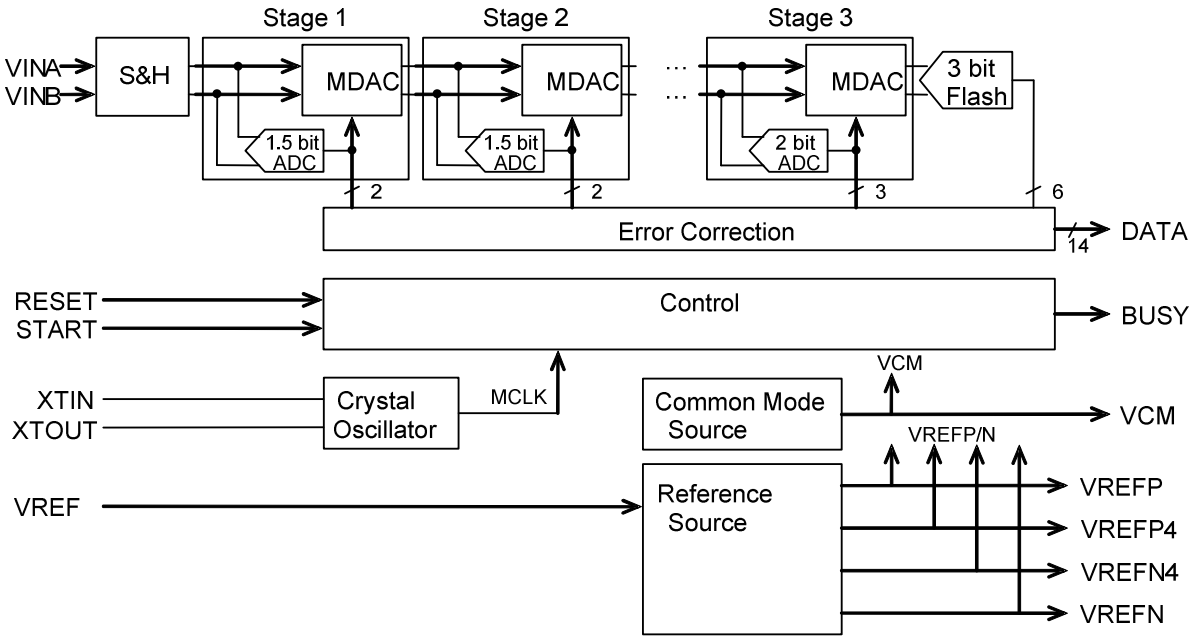
Analog IP Cell

Pipeline ADC 14Bit

XH018

General Description

This cell is a differential, fast 14 bit Pipeline ADC. First stage has the Sample&Hold function and performs a single-ended to differential conversion when required. Differential or single-ended signals can be fed into VINA and VINB. For single-ended signals one input has to be connected to VCM. The supply voltage is used as reference. With the Pin VREF the internal reference can be overwritten. The reference is generated as follows: VREFP = VCM + VREF and VREFN = VCM – VREF,
VCM = VDD/2, is internally generated. The conversion rate is 6.7 MSps @ 20 MHz in continuous mode. The delay between input sampling and data output ist 25 clock cycles.



Ratings, Parameters and Conditions

Electrical Parameters						
Parameter / Condition	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Comment**
Operating Temperature	T_{OP}	-40		85	℃	
Supply Voltage	V_{DD}	3.0	3.3	3.6	V	
Current Consumption	I_{DD}		70	100	mA	at 20 MHz
Clock Frequency	f_{CLK}		20	40	MHz	
Conversion rate	f_{SAMPLE}		f_{CLK} / 3		MHz	
Pipeline Delay	t_{PD}		25 / f_{CLK}		s	
Common Mode Voltage	V_{VCM}		V_{DD} / 2		V	
Int. Reference Voltage	V_{VREF}		V_{DD} / 2		V	
Resolution	RES		2 * VREF / 16384		V	
Differential Nonlinearity	DNL	-1.5		+1.5	LSB	VREF = VDD/2
Integral Nonlinearity	INL	-2.5		+2.5	LSB	VREF = VDD/2
Input Voltage	V_{IN}	0		V_{DD}	V	
Startup Time	T_{SU}			50	µs	