Analog IP Cell
Two Stage 12 bit SAR ADC
ADC12b – XFAB XH018

SERMA
PRODUCTIVITY ENGINEERING

General Description

This cell is a ratiometric operating and very fast 12 bit SAR ADC comprising of a two stages. The first stage converts one bit in advance which is used for digital error correction. The supply voltage is used as reference. The conversion time is about 3.5µs @ 12 MHz in continuous mode.

Ratings, Parameters and Conditions

Absolute Maximum Ratings						
Parameter / Condition	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Comment**
Operating Temperature	T_{OP}	-40		120	°C	
Supply Voltage	V_{DD}	-0.3		3.6	V	
Input Voltage	V_{IN}	-0.3		$V_{DD}+0.7$	V	
Output Voltage	V_{OUT}	-0.3		$V_{DD}+0.7$	V	

Electrical Parameters						
Parameter / Condition	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Comment**
Operating Temperature	T_{OP}	-40		85	°C	
Supply Voltage	V_{DD}	2.7	3.0	3.3	V	
Current Consumption	I_{DD}		0.8	1	mA	12 MHz operation
Clock Frequency	f_{CLK}	1	12	16	MHz	
Conversion Cycle	N_{CYC}		40		Clocks	
Int. Reference Voltage	V_{REF}		$V_{DD30} / 2$		V	
Resolution	RES		$V_{DD30} / 4096$		V	
Differential Nonlinearity	DNL	-1.5		+1.5	LSB	
Integral Nonlinearity	INL	-2.5		+2.5	LSB	
Input Voltage	V_{IN}	0		V_{DD30}	V	
Startup Time	T_{SU}			50	µs	

Interface and Symbol

IO-Description			
Interface	**I/O**	**Function**	**Comment**
IBN5U	input	bias current input	~5uA
VIN	input	input voltage	
CLK	input	clock frequency	
ENABLE	input	enable	
DATA	output	data out	
SOC	input	start of conversion	
EOC	output	end of conversion	
SCE	input	scan path enable	low if unused
SCI	input	scan path in	low if unused
SCO	output	scan path out	
VDD30, VSS	power	supply voltage	


```
        SAR_ADC_TOP
  VDD30 DATA<11:0>
  VSS

  IBN5U

  VIN

  CLK

  SOC            EOC

  SCE
  SCI            SCO

  ENABLE
```