Digital IP Cell

Serial Peripheral Interface
SPI-S

SERMA PRODUCTIVITY ENGINEERING

General Description

The PE SPI_Slave is a Serial Peripheral Interface soft-macro - IP block that can be implemented in digital or mixed signal ASIC designs. The SPI interface and its various transfer modes for data transfer is a simple and flexible way to transfer data in multi IC-systems in SPI master/slave configuration.
The PE SPI_Slave is compliant with the standard definition of the SPI-protocol. For a customisation the soft-macro is flexible. The clock speed is mainly determined by applied technology and peripheral circuitry and is specified in the range of 1 – 60 MHz.
VHDL synthesized gate count is in the order of 120 equivalent gates.
The range of applications is wide. For example from simple data transfers to complete ASIC configuration purposes employing sets of addresses and dedicated registers. The internal structure allows a data width of 24 or 16 Bits in write or read mode respectively.
All output signals are fully decoded and timed for synchronous control.

In this version the PESPI_Slave transmits 24 Bit per SPI frame. The first 8 bit are mapped to a dedicated address register and the next 16 bit are mapped to the data payload register. After reception of 8 bits address code the soft-core sends 16 bits of data synchronously from the internally selected register (full duplex communication).

Ratings, Parameters and Conditions

Description: VHDL, EDIF
Parameters: 24 bits per SPI cycle
- 8 bits address send (generic changeable)
- 16 bits data send / receive (generic changeable)

Frequency range: 1 – 60 MHz
Dimension / Range: 0,06 mm^2 (0,6µm Standard Cell CMOS Technology)
Number of ports: 47

IO-Description

Interface	I/O	Function
RESET_NI	Input	Reset low active
CLK_I	Input	Internal Clock for synchronisation
SPI_SEL_I	Input	Select SPI low active
SPI_SCLK_I	Input	Transfer clock for SPI
SPI_MOSI_I	Input	Serial data master out slave in
SPI_MISO_O	Output	Serial data master in slave out
SPI_EN_O	Output	Synchronous end of transfer
SPI_ADR_O	Output	Parallel address bus
SPI_DAT_I	Input	Parallel data bus in
SPI_DAT_O	Output	Parallel data bus out

Symbol