Digital IP Cell

Pulse Width Modulator

PWM1

SERMA PRODUCTIVITY ENGINEERING

General Description

Depending on a parallel bit word at the input this circuit cell generates a number of high pulses within a given time frame on the output. The cell is generic and the input word width can be defined prior to synthesis. The higher the value the more pulses per time frame. This can then be used with an RC low pass filter and an OTA to generate an equivalent analogue output voltage. The circuit is very small and can easily be adapted to any type of application since it is VHDL coded and is available in vhdl, verilog or edif netlist format. The amount of high-level peaks is equal to the input word size after 256 clock periods.

Ratings, Parameters and Conditions

Parameter / Condition	Symbol	Min	Typ.	Max	Unit	Comment
Electrical Parameters						
Conversion time	T_{conv}		11		Clk periods	First result after data load
Clock frequency	F_{clk}	1	8	100	MHz	Depending on application and technology
Gate count			<100			equivalent gates (for 8 bit word)

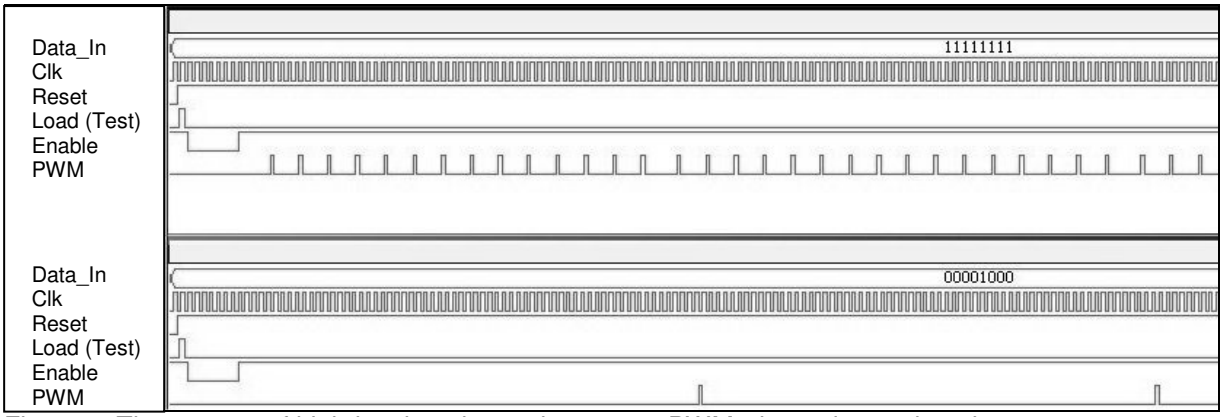

Figure 1: The amount of high-level peaks on the output “PWM” depends on “data_in”

IO-Description

Interface	I/O	Function	Comment
Vdd	Input	Supply	
Gnd	Input	Supply	
Data_in[0..7]	Input	Data input	
PWM_Out	Output	PWM Output	
Clk	Input	Clock	
Reset	Input	Reset	
Enable	Input	Enable	Conversion enable

Symbol and external Component Schematic