Analog IP Cell

Phase Locked Loop

PLL1 XB06

SERMA PRODUCTIVITY ENGINEERING

General Description

The Phase Locked Loop PLL1 is designed to operate as a controllable clock source. Primarily it can be used for clocking higher speed digital cores. It generates a square wave signal having an integer frequency multiple of a supplied reference signal (IntegerN PLL). This feature admits the use of low speed external quartz crystals as clock reference and clocking the internal circuitry at a higher rate. Because of the controllable ratio of input and output frequency, the speed of the clocked core can be adjusted. This gives the chance to scale the processing power to current requirements to achieve the best possible performance in relation to consumed power.

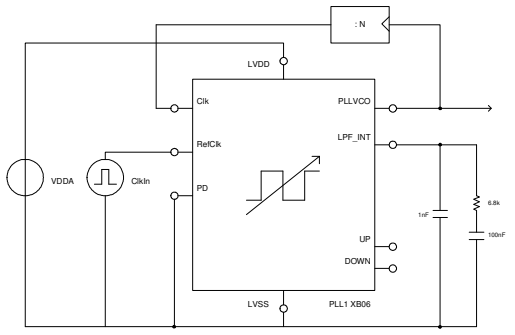
Ratings, Parameters and Conditions

Parameter / Condition	Symbol	Min	Typ.	Max	Unit	Comment
Electrical Parameters:						
Supply Voltage	V_{dd}	4.75	5	5.25	V	
Supply Current	I_{dd}		1500		uA	100MHz VCO - frequency
VCO Frequency	F_{VCO}	15		150	MHz	
Output Duty Cycle		40	50	60	%	
PLL Stable Time	T_{PLLSTB}		100		us	
Jitter	T_J		100		ps	
Rise Time	T_R		1.5		ns	
Fall Time	T_F		1.3		ns	
Absolute Maximum Ratings:						
Operating Temperature	T_{range}	-40		120	℃	
Supply Voltage	V_{dd}	-0.3		7	V	
Input Voltage	V_{in}	-0.3		V_{dd}+0.7		
Output Voltage	V_{out}	-0.3		V_{dd}+0.7		
Operating Conditions:						
Ambient Temperature	T_{amb}	-20	27	80	℃	

IO-Description

Interface	I/O	Function	Comment
LVDD	Input	Supply	
LVSS	Input	Supply	
PD	Input	Power Down	High active
REFCLK	Input	Clock Input	
CLK	Input	Divided PLL Clock	
PLLVCO	Output	PLL Clock Output	
LPF_INT	InOut	Loop Filter	
UP	Output	Charge Pump Up	
DOWN	Output	Charge Pump Down	

Symbol and external Component Schematic



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