

#### General Description

CapSense Megacell is a scalable capacitive sensor signal conditioning circuit IP.

It can be used for intelligent push-button sensors e.g. for remote controls.

The capacitance increases with the touch of the button by a factor depending on the sensor material (e.g.  $3 * C_{\text{sensor}}$ ). It has all necessary column driving circuitry as well as row readout amplifiers, filters and ADC circuitry. The sensor array itself can be a flexible polymer based sensor array with a resolution as high as 500dpi. A column driver drives a sine wave signal coming from an integrated signal generator while all other columns are tied to virtual ground. All rows are then scanned at the same time. The value is filtered and converted into a digital signal. The result can be read out through a parallel bus at a resolution of 8 bit. The controller sequence allows to scan a whole sensor field several times a second, depending on matrix size, frequency and the single push button/sensor field capacitance. The circuit system is highly flexible (CMOS06, BiCMOS035) and can be designed into any ASIC requirement.

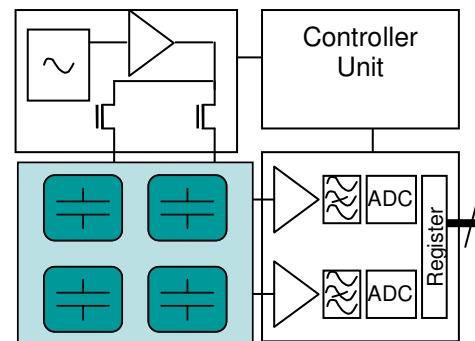
#### Ratings, Parameters and Conditions

Parameter / Condition	Symbol	Min	Typ.	Max	Unit	Comment
Electrical Parameters						
<b>Sensor Array</b>						
CapSense Array size	$N_{\text{array}}$	2x2		100x100		Can be either pixels or touch buttons
Sensor capacitance	$C_{\text{sensor}}$	3		1000	fF	adjustable to any sensor field
Pixel clock	$F_{\text{pixel}}$		7.3728		MHz	representative value/adjustable
Line sync clock	$F_{\text{line}}$		7.2		kHz	representative value/adjustable
Frame sync clock	$F_{\text{frame}}$		8.44595		Hz	representative value/adjustable
<b>Row Signal Amplifier Unit</b>						
settling time	$t_{\text{START}}$			8	us	
counter delay	$t_{\text{DZ}}$			2	ns	after clock posedge
reset delay	$t_{\text{R}}$			2	ns	after reset negedge
data preload time	$t_{\text{DT}}$	2			ns	
data hold time	$t_{\text{DH}}$	2			ns	
filter time constant	$T_{\text{FILT}}$		1000		ns	analog row filter
bandwidth I/U converter	$BW_{\text{I/U}}$	10			MHz	determines array frequency
<b>Column Driver Unit</b>						
linear range column driver	$V_{\text{shift}}$	1		4	V	
shift frequency	$f_{\text{shift}}$		10		kHz	column to column
Stimuli clock frequency	$F_{\text{stim}}$	1	10	12	MHz	

#### IO-Description

Interface	I/O	Function	Comment
Vdd	Input	Supply	
Gnd	Input	Supply	
Array_c[0..n]	Output	driver	Array columns
Array_r[0..n]	Input	readout	Array rows
clk	Input	Clock	
reset	Input	Reset	Global reset
ena	Input	Enable	
D_out[0..7]	Output	Data	Output data
Setup[0..2]	In/out	Serial port	Progr./Test register

#### Symbol and external Component Schematic



Dieses Projekt wird mit Mitteln des Europäischen Sozialfonds (ESF) gefördert. Es erzeugt einen gemeinschaftlichen Mehrwert „Investition in Ihre Zukunft“.