

# Analog IP Cell

## 13Bit Analog Digital Converter

### SARADC13XB06



#### General Description

This 13Bit successive approximation analog to digital converter employs a charge scaling network to convert unipolar input voltages to a digital data word within 33µs with a resolution of 13Bit. To achieve this high accuracy and to keep test costs down, the converter is able to do a self calibration cycle for capacitor mismatch balancing. By this cycle, a correction word for every Bit is measured by a digital to analog converter having only 8Bit of resolution, which is used for error correction during normal operation.

#### Ratings, Parameters and Conditions

| Parameter / Condition        | Symbol      | Min  | Typ.    | Max          | Unit | Comment                 |
|------------------------------|-------------|------|---------|--------------|------|-------------------------|
| Electrical Parameters        |             |      |         |              |      |                         |
| Supply voltage               | $V_{dda}$   | 4.75 | 5       | 5.25         | V    |                         |
| Operating Temperature        | $T_{range}$ | -20  |         | 85           | °C   |                         |
| Supply current analog        | $I_{dda}$   |      |         | 3            | mA   |                         |
| Supply current digital       | $I_{dd}$    |      |         | 2            | mA   |                         |
| Resolution                   | N           |      | 13      |              | Bit  |                         |
| Analog Ground voltage        | $V_{GNDA}$  |      | 2.5     |              | V    |                         |
| Reference voltage            | $V_{ref}$   | 1    |         | 2.5          | V    | measured to $V_{GNDA}$  |
| Duration of conversion       | $T_{conv}$  |      | 33      |              | µs   | using 8MHz main clock   |
| Duration of calibration      | $T_{cal}$   |      | 150     |              | µs   | using 8MHz main clock   |
| Differential linearity error | $ADC_{DNL}$ |      | +/- 1/4 | +/- 3/4      | LSB  | after calibration cycle |
| Integral linearity error     | $ADC_{INL}$ |      |         | +/- 2        | LSB  | after calibration cycle |
| Offset error                 | $ADC_{Off}$ |      | 1       | 3            | LSB  | after calibration cycle |
| Absolute Maximum Ratings     |             |      |         |              |      |                         |
| Storage Temperature          | $T_{range}$ | -40  |         | 125          | °C   |                         |
| Supply Voltage               | $V_{dd}$    | -0.3 |         | 7            | V    |                         |
| Input Voltage                | $V_{in}$    | -0.3 |         | $V_{dd}+0.7$ |      |                         |
| Output Voltage               | $V_{out}$   | -0.3 |         | $V_{dd}+0.7$ |      |                         |

#### IO-Description

| Interface      | I/O    | Function          | Comment |
|----------------|--------|-------------------|---------|
| CLK            | Input  | digital clock     |         |
| POR            | Input  | power on reset    |         |
| SOC            | Input  | start conv.       |         |
| CALIB          | Input  | start calib.      |         |
| EOC            | Output | end of conv.      |         |
| Vref           | Input  | reference voltage |         |
| Vin            | Input  | input voltage     |         |
| B_out[0..12]   | Output | ADC result        |         |
| GND, GNDA, VDD | Input  | voltage supply    |         |

#### Symbol

