PE5001 Analog Multiplexer

Application Note

PE5001 as driver for dot matrix-LCDs

SERMA PRODUCTIVITY ENGINEERING

Dot-Matrix LCD driver

An LCD matrix control circuit requires at least two PE5001 and a controller. With two ICs a matrix with a maximum size of 100x100 dots can be driven. Larger displays can be driven by more Multiplexers accordingly. This is only limited by the I/O speed of the microcontroller. Smaller displays can be driven as well by not using outputs of the PE5001.

Three different voltages have to be supplied to the dot matrix LC display. A simplified system configuration example for a 3x3 matrix is presented in Figure 1. Other configurations are feasible using more or less I/O ports of the controller.

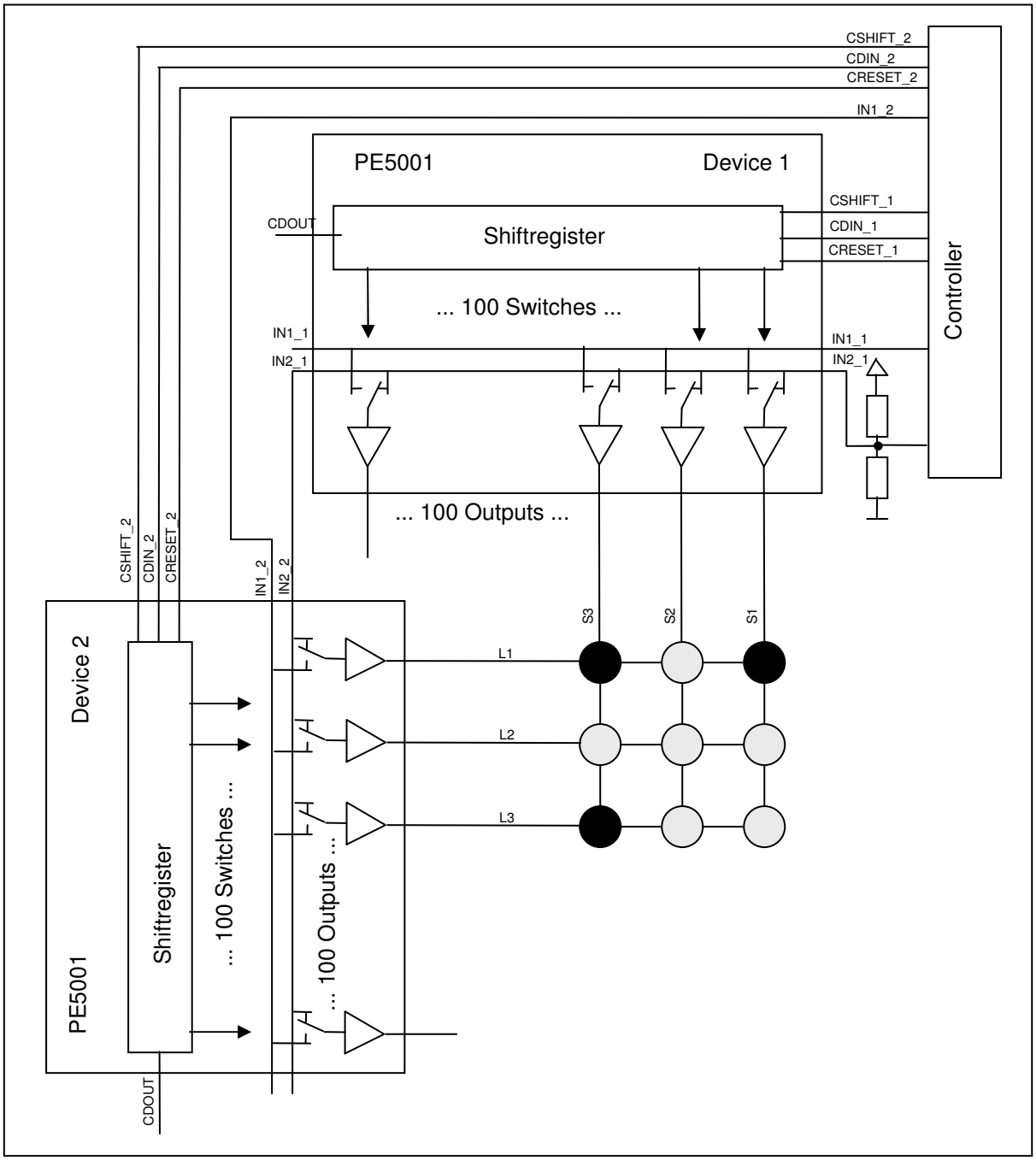


Figure 1: System configuration example

LCD drive mode waveforms

The line and segment driver waveforms are shown in Figure 2.

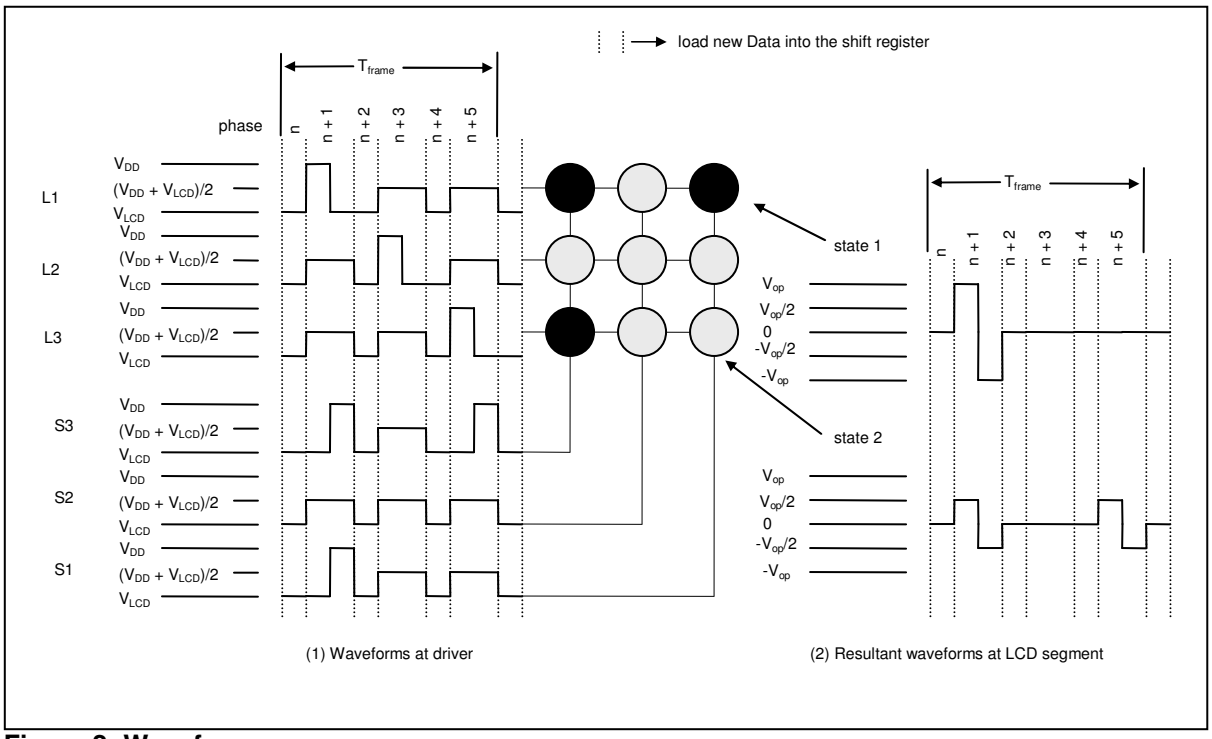


Figure 2: Waveforms

A simplified example of the condition of the input signals during the respective phases can be found in Table 1.

phase	n	n + 1	n + 2	n + 3	n + 4	n + 5
CSHIFT_1	_⎍⎍⎍	⎯⎯⎯⎯⎯	_⎍⎍⎍	⎯⎯⎯⎯⎯	_⎍⎍⎍	⎯⎯⎯⎯⎯
CDIN_1	…101	-	…000	-	…100	-
CSHIFT_2	⎍	⎯⎯⎯⎯⎯	⎍	⎯⎯⎯⎯⎯	⎍	⎯⎯⎯⎯⎯
CDIN_2	…001	-	…010	-	…100	-
IN1_1	V_{LCD}	V_{DD}- V_{LCD}- ⎍	V_{LCD}	V_{DD}- V_{LCD}- ⎍	V_{LCD}	V_{DD}- V_{LCD}- ⎍
IN1_2	V_{LCD}	V_{DD}- V_{LCD}- ⎍	V_{LCD}	V_{DD}- V_{LCD}- ⎍	V_{LCD}	V_{DD}- V_{LCD}- ⎍
IN2_1= IN2_2	V_{LCD}	$(V_{DD}+V_{LCD})/2$	V_{LCD}	$(V_{DD}+V_{LCD})/2$	V_{LCD}	$(V_{DD}+V_{LCD})/2$

Table 1: Input signals in correspondence to phases

Shift register

The input data stream for the shift register is defined by pin 'CDIN'. The register is shifted step by step in a serial manner with a pulse on 'CSHIFT'. Pin 'CRESET' sets all registers to '0'. The shift register controls the analog switches. A binary '1' in a register connects the output driver to IN1. A binary '0' connects the output driver to IN2.

Segment outputs

The first PE5001 drives up to 100 segment inputs. They have to be connected directly to the LCD. The segment input voltages are in accordance with the two analog input signals at IN1_1 and IN2_1 and with the data in the shift register. A binary '1' in a register connects an output driver to IN1.
A binary '0' connects the output driver to IN2. The controller has to ensure that the voltage levels of IN1_1, IN2_1, IN1_2 and IN2_2 are all the same while the data stream is being shifted. In this short time no LCD dot will be active.

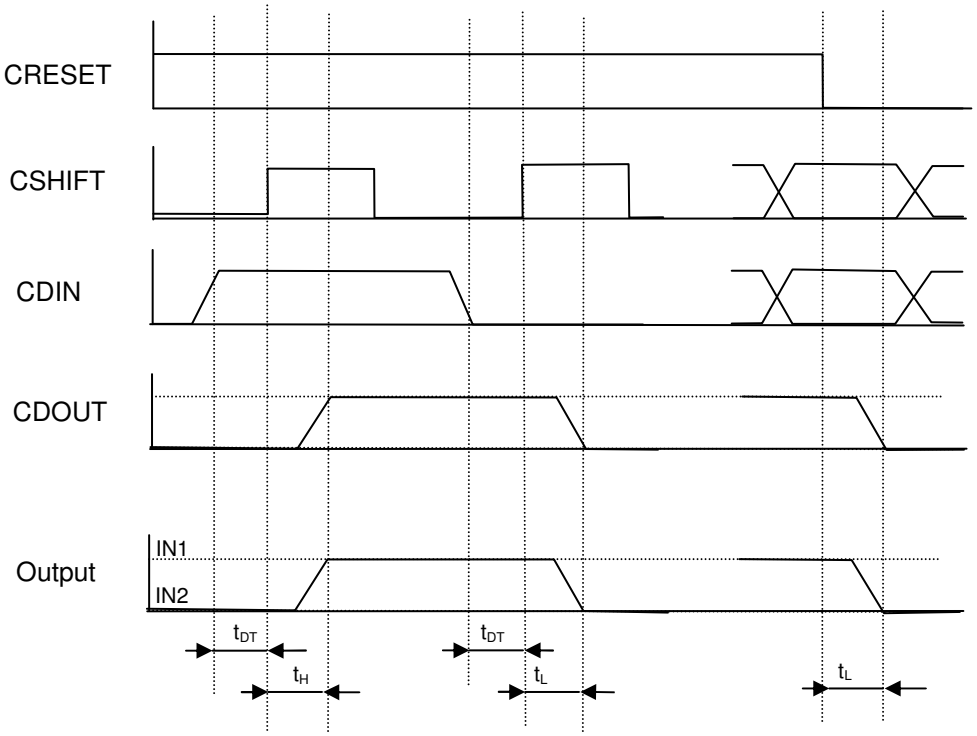
Line outputs

The second PE5001 drives the lines (backplanes) and has to be connected directly to the LCD. The line output signals are generated in accordance with the two analog input signals at IN1_2 and IN2_2 and with the data resident in the shift register. A binary '1' in a register connects the output driver to IN1. A binary '0' connects the output driver to IN2. Side by side lying outputs can be tied together to give enhanced drive capabilities. The binary '1' in device 2 can shift with one clock at CSHIFT_2 to switch on the next line. When two outputs are tied together the two binary ones must be pushed with two clocks on CSHIFT_2. During shifting, the voltage levels of IN1_1, IN2_1, IN1_2 and IN2_2 should be alike.

Table 2 : Dynamic properties (V_{DD}=5V,T=27°C)

Parameter	Symbol	Min	Typ	Max	Unit
turn on / high time	t_H			2	ns
turn off / low time	t_L			2	ns
data pre-charge time	t_{DT}	2			ns
CSHIFT frequency	f_C		10		MHz

Timing Diagram



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This project was supported by Award No. 2005-IJ-CX-K067 awarded by the National Institute of Justice, Office of Justice Programs, US Department of Justice. The opinions, findings, and conclusions or recommendations expressed in this publication/program/exhibition are those of the author(s) and do not necessarily reflect the views of the Department of Justice.