Analog IP Cell

Two Stage 12 bit SAR ADC

ADC12b – XFAB XH035

SERMA PRODUCTIVITY ENGINEERING

General Description

This cell is a ratiometric operating and very fast 12 bit SAR ADC comprising of two stages. The second stage converts one bit in advance which is used for digital error correction. The reference voltage is provided by an external bandgap cell. The conversion time is about 3.5µs @ 12 MHz in continuous mode.

Ratings, Parameters and Conditions

Absolute Maximum Ratings						
Parameter / Condition	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Comment**
Operating Temperature	T_{OP}	-40		120	℃	
Supply Voltage	V_{DD}	-0.3		3.6	V	
Input Voltage	V_{IN}	-0.3		V_{DD}+0.7	V	
Output Voltage	V_{OUT}	-0.3		V_{DD}+0.7	V	

Electrical Parameters						
Parameter / Condition	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Comment**
Operating Temperature	T_{OP}	-40		85	℃	
Supply Voltage	V_{DD}	3.0	3.3	3.6	V	
Current Consumption	I_{DD}		0.4	0.6	mA	12 MHz operation
Clock Frequency	f_{CLK}	1	4	12	MHz	
Conversion Cycle	N_{CYC}		40		Clocks	
External Reference Voltage	V_{REF}	1.1	1.2	1.5	V	
Internal low Reference	V_{REFN}		V_{REF}-V_{REF}/3		V	
Internal high Reference	V_{REFP}		$V_{REF+}V_{REF}$/3		V	
Resolution	RES		V_{REF} / 6144		V	
Differential Nonlinearity	DNL	-1.0		+1.0	LSB	
Integral Nonlinearity	INL	-2.5		+2.5	LSB	
Input Voltage	V_{IN}	V_{REFN}		V_{REFP}	V	
Startup Time	T_{SU}			50	µs	

Interface and Symbol

IO-Description			
Interface	**I/O**	**Function**	**Comment**
IBP5U	output	bias current sink	~5uA
VIN	input	input voltage	
VREF	input	reference voltage	
CLK	input	clock frequency	
ENABLE	input	enable	
DATA	output	data out	
SOC	input	start of conversion	
EOC	output	end of conversion	
EOS	output	end of sample	
VDD, VSS	power	supply voltage