

### General Description

This digital-to-analog converter employs R2R ladder architecture in a current scaling network. Binary weighted currents are produced and accumulated at one of the two output networks. Assignment of the currents is done by CMOS decoding circuit. The output voltage is buffered by a low impedance CMOS follower. The cell is designed for high accuracy and best resistor matching. The upper and lower input reference voltage is programmable.

### Ratings, Parameters and Conditions

Parameter / Condition	Symbol	Min	Typ.	Max	Unit	Comment
Electrical Parameters						
Supply voltage	$V_{dda}$	4.75	5	5.25	V	
Supply current	$I_{dda}$			1	mA	
Resolution	N		10		Bit	
Upper reference voltage level	$V_{refhigh}$	3		4.9	V	programmable
Lower reference voltage level	$V_{reflow}$	0.1		2	V	programmable
Reference voltage input current	$I_{vref}$			500	uA	
Max. output current	$I_{vdacmax}$	1			mA	
Output voltage settling time	$T_{voutset}$			50	ns	
LSB voltage	$V_{lsb}$	$(V_{refhigh} - V_{reflow}) / 2^N$			V	
Differential linearity error	$DAC_{DNL}$		$\pm 1/4$	$\pm 3/4$	LSB	
Integral linearity error	$DAC_{INL}$			$\pm 2$	LSB	
Offset error	$DAC_{Off}$		1	3	LSB	
Gain error	$DAC_{Gain}$		2	8	LSB	
Operating Temperature	$T_{range}$	-40		120	°C	
Supply Voltage	$V_{dd}$	-0.3		7	V	
Input Voltage	$V_{in}$	-0.3		$V_{dd}+0.7$		
Output Voltage	$V_{out}$	-0.3		$V_{dd}+0.7$		
Supply Current	$I_{dd}$			50	mA	
Ambient Temperature	$T_{amb}$	-20	27	80	°C	
Supply Voltage	$V_{dd}$	4.75	5	5.25	V	

### IO-Description

Interface	I/O	Function	Comment
Vrefhigh	Input	Upper reference	One LSB $(V_{refhigh} - V_{reflow}) / 2^{10}$
Vreflow	Input	lower reference	
Bin	Input	data	
DACout	Output	buffered output	
GNDa	Input	analogue ground	
VDDa	Input	analogue supply	

### Symbol

