Analog IP Cell

Power-on-Reset

POR XB06

SERMA PRODUCTIVITY ENGINEERING

General Description

Most of today's integrated circuits are working in a mixed signal environment containing digital and analogue core cells. Because of the need of predefined conditions after start-up, the digital core has to be reset after power up.
Power-On-Reset (POR) is being implemented to avoid malfunction of the digital core in some operating conditions. This circuit checks whether the supply voltage is in a range ensuring a defined mode of operation, which is predominantly defined by the analogue circuitry. This behaviour is important for slow power supply voltage transitions. Then the POR guarantees a defined reset delay after power up to ensure all digital parts are in an operating state and are able to react properly on a clock. This behaviour is important for fast supply voltage transitions.

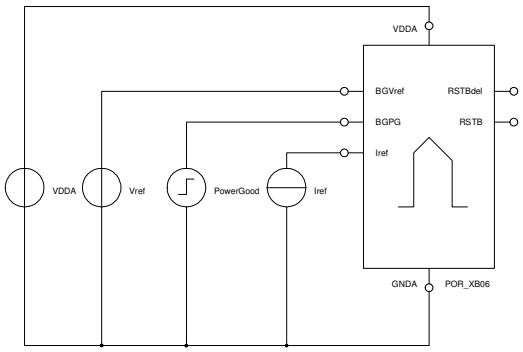
Ratings, Parameters and Conditions

Parameter / Condition	Symbol	Min	Typ.	Max	Unit	Comment
Electrical Parameters:						
Supply Voltage	V_{dd}	4.75	5	5.25	V	
Supply Current	I_{dd}	55	70	90	uA	
reset low -> high threshold voltage	V_{RLH}	3.9	3.94	4	V	
reset high -> low threshold voltage	V_{RHL}	3.4	3.6	3.7	V	
reset low -> high delay (RSTB -> RSTBDEL delay)	T_{DLH}	200	380	910	us	
reset low -> high delay (RSTB -> RSTBDEL delay)	T_{DHL}	170	360	970	us	
Absolute Maximum Ratings:						
Operating Temperature	T_{range}	-40		120	℃	
Supply Voltage	V_{dd}	-0.3		7	V	
Input Voltage	V_{in}	-0.3		V_{dd}+0.7		
Output Voltage	V_{out}	-0.3		V_{dd}+0.7		
Operating Conditions:						
Ambient Temperature	T_{amb}	-20	27	80	℃	

IO-Description

Interface	I/O	Function	Comment
VDDA	Input	Supply	
GNDA	Input	Supply	
BGVREF	Input	reference voltage	nominal 1.22V
BGPG	Input	power good signal bandgap reference	active high logic
IREF	Input	bias current input	
RSTB	Ouput	reset signal	low active logic
RSTBDEL	Output	delayed reset signal	low active logic

Symbol and external Component Schematic



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