

Features

- Programmable Sinusoidal frequency generator
- 10 bit DAC
- Crystal oscillator
- analogue Reference voltage generators
- SPI
- Interfaces to PE5001 and PE5002

Applications

- capacitive sensor signal acquisition
- Touch Screen / Touch Buttons
- Fingerprint Sensor (capacitive arrays)
- laboratory bio-chemical cell growth monitoring
- permittivity based liquid analysis and flow monitoring

General Description

This PE5003 is part of the PE500x Capacitive Sensor Solution. It can also be used for stand-alone applications where some or all functions might be required. The main task in conjunction with the PE500x Capacitive Sensor Solution is to control all functions of the PE5001 Analogue Multiplexer IC and the PE5002 100-input capacitive sensor signal conditioner IC. It features analogue reference voltage generators, crystal clock generator and clock driver, a 10bit DAC (Digital Analogue Converter) and a sine-wave signal generator. Most of the functionality is programmable through the SPI and can be adjusted to fit different system configurations, sensor array sizes and width and length of the array as well a different capacitances of the capacitive sensors.



Figure 1 - Block diagram



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1 Revision History

Version	Date	Changes	Page
Initial Version V1.0			



2 Ratings

2.1 Absolute Maximum Ratings

Table 1 -

Parameter	Symbol	Min	Тур	Max	Unit	Notes
Operating Temp.	T _{range}	-40		120	°C	
Supply voltage	V _{dd}	-0.3		7	V	
Input voltage	V _{in}	-0.3		Vdd+0.7		
Output voltage	V _{out}	-0.3		Vdd+0.7		
Supply current	I _{dd}			50	mA	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2.2 Operating Conditions

Table 2 -

Parameter	Symbol	Min	Тур	Max	Unit	Notes
Operating Temp	T _{amb}	-20	27	85	S	
Supply voltage digital	V _{dd}	4.75	5	5.25	V	
core						
Supply voltage	V _{dda}	4.75	5	5.25	V	
analogue core						
Supply current	I _{dd} + I _{dda}		30		mA	

2.3 Detailed Electrical Ratings

Table 3 - Static Operating Conditions (T_{amb} = 27 °C; V_{dda} = 5 V, unless otherwise noted):

Parameter	Symbol	Min	Тур	Max	Unit	Notes
Input voltage high	V _h	4			V	
Input voltage low	VI			1	V	

Table 4 - Dynamical Operating Conditions

(800 sensor columns, $T_{amb} = 27 \text{ °C}$; $V_{dda} = 5 \text{ V}$, unless otherwise noted):

Parameter	Symbol	Min	Тур	Max	Unit	Notes
power up time	T _{startup}			5	ms	
DAC reference voltage settling time	T _{voutset}			50	ns	
Clock frequency digital	F _{dig}		7.3728		MHz	
Flag shift frequency column control ASICs	F _{cshift}		6.75676		kHz	
Stimuli clock frequency	F _{stim}		10		MHz	
Stimuli clock rise time	T _{stimrise}		50		ns	V_{mid} -1.5V ~ V_{mid} +1.5V
Stimuli clock fall time	T _{stimfall}		50		ns	V_{mid} +1.5V ~ V_{mid} -1.5V
Analogue to digital conversion time	T _{daclock}		135.742		ns	
Serial interface shift	F _{sshift}		7.3728		MHz	
frequency						
Pixel clock	F _{pixel}		7.3728		MHz	
Line sync clock	F _{line}		7.2		kHz	
Frame sync clock	F _{frame}		8.44595		Hz	



3 Analogue Circuit Overview

3.1 Bandgap Reference

The Bandgap reference circuit generates the absolute reference voltage level. This voltage is used as scaling factor for digital to analogue conversion. The DAC maximum output voltage is $(V_{refhigh} - V_{reflow}) - V_{lsb}$ where $V_{lsb} = (V_{refhigh} - V_{reflow}) / 1024$.

3.2 DAC Reference Generator

The DAC reference generator is responsible for setting the digital to analogue converters maximum and minimum output voltage. The maximum reference voltage is derived out of the bandgap voltage. The upper and lower reference voltage is generated by two SPI controlled R2R DACs with 4bit resolution.

Table 5 – Electrical Parameters

Parameter	Symbol	Min	Тур	Max	Unit	Notes
Lower reference voltage level	V _{reflow}	0.5		2	V	actual value according SPI register settings
Upper reference voltage level	V _{refhigh}	3		4.5	V	actual value according SPI register settings
Power supply rejection ratio	PSRR _{vref}	40			dB	
Output Current	I _{vref}			3	mA	

3.3 Virtual Ground Supply

The virtual ground supply block is used for creating a signal ground level at the midpoint of the analogue supply voltage. This potential is essential for sensor matrix biasing (the matrix, inactive columns and the row signal conditioner's input circuits are tied and referenced to this level avoiding DC current flow through the sensor matrix because of finite isolation resistances). Signal ground is also the reference for the matrix stimulating sine wave generator, oscillating around this voltage level. The produced voltage level is buffered with a low impedance follower to "SDC" to make virtual ground independent of external effects.

Table 6 – Electrical Parameters

Parameter	Symbol	Min	Тур	Max	Unit	Notes
Output voltage	V _{virtgnd}		0.5*Vdd		V	
Maximum output	I _{virtgnd}			1	mA	
current	-					
Output resistance				2	Ohm	
Power supply rejection	PSRR _{virt}	10			dB	
ratio						



3.4 Crystal Oscillator

The digital core of the system controller's circuitry is a clock synchronous design and needs a master clock for operation. This can be supplied externally e.g. from a microcontroller clock source via "XTin". The PE5003 also has an integrated oscillator having a nominal frequency of 7.3728 MHz, which is defined by an external frequency determining crystal between "XTin" and "XTout ". Values diverging from nominal frequency can be used for testing purposes but result in not specified frame and pixel rates.

Table 7 – Electrical Parameters

Parameter	Symbol	Min	Тур	Max	Unit	Notes
Output frequency	F _{diq}	4	7.3728	10	MHz	Crystal frequency
Rise Time	T _{rise}			5	ns	10% Vdd ~ 90% Vdd
Fall Time	T _{fall}			5	ns	90% Vdd ~ 10% Vdd
External capacitors	C _{cosc}		22		pF	

Block Schematic and External Component Schematic:



3.5 Programmable Sinusoidal Oscillator

The capacitive sensor matrix has to be stimulated by a frequency generator for determination of the actual capacitance of a particular sensor cell. The PE5003 provides a sine wave signal having a nominal frequency of 10 MHz and an amplitude of about 1.5 V. The operating frequency can be adjusted in a predefined range by setting the SPI register bits (4 bit).

Parameter	Symbol	Min	Тур	Max	Unit	Notes
Output frequency	F _{stim}	1		10	MHz	tuning range
Output amplitude	V _{stim}		3		V	balanced around analogue mid voltage



3.6 Digital-to-Analogue Converter

An analogue-to-digital conversion has to be performed for every line in the row signal conditioner PE5002. The PE5002 uses a comparator per channel and a reference voltage for AD conversion. This reference voltage is generated by a digital to analogue converter in the PE5003. Please refer to the *"Application Note - PE5002 controlled by an external microcontroller"* when not using the PE5003. The output voltage is buffered by low impedance follower for distributing it over the whole sensor matrix.

Parameter	Symbol	Min	Тур	Max	Unit	Notes
Resolution	Ν		10		Bit	
Upper reference	V_{refhigh}	3		4.9	V	actual value according SPI
vollage level				-		register settings
Lower reference	V _{reflow}	0.1		2	V	actual value according SPI
voltage level						register settings
Reference voltage	I _{vref}			1	mA	
input current						
Max. output current	I _{vdacmax}	1			mA	
Output voltage settling	T _{voutset}			50	ns	
time						
LSB voltage	V _{Isb}		(V _{refhigh} –		V	
			V _{reflow}) /			
			1024			
Differential linearity	DAC		+-1/4	+- 3/4	LSB	
error						
Integral linearity error	DACINL			+-2	LSB	
Offset error	DAC _{Off}		1	3	LSB	
Gain error	Dac _{Gain}		2	8	LSB	

Table 9 – Electrical Parameters



4 Digital Circuit Overview



In this flow chart there are two parallel processes. The first process is the sensor data read-in (converted to digital domain by the PE5002 row sensor signal conditioners ADCs). It starts by enabling a counter (Cnt1 from 0 to 1023) being the input data for the PE5003 digital to analogue converter. Converted to analogue domain, this signal forms a sawtooth voltage reference. Besides this measurement process, data transfer to a host PC takes place controlled by the transfer counter (Cnt2, counting from 0 to 1023 as well). Because of the Cnt2's fixed architecture, the data transfer rate is independent from actual matrix dimensions. Data of sensor rows, which are not physically present and so do not generate a sensor signal, are transferred as logical zero. During this procedure, the Main Control starts the next counting process. The measurement process is triggered by the signal SNAP und ended by the read in flag CFlagin.



4.1 Functional Description – Digital Block Diagram

The diagram shows the general block structure with all digital components of the PE5003.



The format of data transfer to a host PC and the interfaces of to PE5001 and PE5002 define the structure of the PE5003. To control the sensor process the PE5003 has two finite state machines. At first, the main control FSM for driving the sensor process. This FSM drives the Reset (low active), controls the scan process and starts a counter (Cnt1) for collection of data and sets an enable to start the data transfer. The write control FSM drives the data transmission to PC and sets a ready signal at the end of one readout cycle. A counter (Cnt2) counts the transmitted data words (10 Bits).

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The integrated SPI-Slave controller allows to access all special function registers of the PE5003 via serial static addressing. One can also read back the states of the counter, FSM and the white balance register. A 16 Bit register allows manipulating the wait cycle for settling time. The SPI registers have the following static structure:

1.	reading/writing	directions:	MSB-first
•••			

2. static sending 24 Bit:

8 Bit address - Bit 7-0 address 16 Bit data

defined in table register width defined

3. Address definition table (Table 10)

Address	Function
76543210	
00011111	Set/Reset Register / Software-Reset
0000001	Calibration Register
0000010	Counter Cnt1 Register initial value
0000011	Counter Cnt2 Register initial value
0000100	State Main Control FSM
0000101	State Write Control FSM
00001001	Program WAIT Counter (0-8191µs with 8MHz), typ. 80µs end value
00001010	Set sine wave generator gain
00010000	Phase coefficient for PE5002 (PCO)
00010001	Gain coefficient for PE5002 (GCO)

4. Data width of registers (Table 11)

Data		· · ·		Function
1 1 1 1	1 1			
5 4 3 2	1 0 9 8	76543	2 1 0	
ХХХХ	ХХХХ	ХХХХ –		Set/Reset Register Counter and Software-Reset
				Calibration Register
upper	lower	Reference		
Ref.	Ref.	of Sine wave		
Voltage	Voltage	Generator		
ХХХХ	ХХ – –			Counter Cnt1 Register
ХХХХ	ХХ – –			Counter Cnt2 Register
ХХХХ	ХХХХ	ХХХХ –		State Main Control FSM
ХХХХ	ХХХХ	ХХХХХ		State Write Control FSM
				settling time for Wait Counter (0-9ns) 80µs on reset
ХХХХ	ХХХХ	ХХХХ –		SinGain(4 bit)
ХХХХХ	X			Phase coefficient data
ХХХХ	Х – – –			Gain coefficient data



4.1.1 SPI register and Programming structure

The module U_PP_SPI_REG1 is an SPI-Slave. This block transfer serial data from PC via SPI-Bus to PE5003 and back. This capture describes the structure and programming SPI commands. The following diagrams are functional descriptions of data transfer from Master SPI.

SPI Write

SPI_SEL		T		I		I					[<u> </u>
SPI_SCLK		Î			Ĺſſſ					ind	inr		
SPI_MOSI		Ť		į		ļ	L			ii			\vdash
SPI_MISO		Ĩ		[1							
START_SPI		Ъţ		-		• 		· · · ·	 				L
PAR_ADRIN	20	03											
PAR_DATAIN	0000	j032	20			1		· ·			 •		
PAR_DATAOUT	0000	-											<u> </u>
-													

PAR_ADR and PAR_DATAIN has been serial transferred with SPI_MOSI (set in Master at falling edge)

SPI READ



PAR_ADR has been serial transferred with SPI_MOSI and an answer comes from SPI_MISO (set in slave with rising edge) to PAR_DATAOUT

SPI WRITE & READ



PAR_ADR and PAR_DATAIN has been transferred serial with SPI_MOSI and an answer comes from SPI_MISO to PAR_DATAOUT



Program (StartUp)-Reset cycle

Every Power-Up sets the digital core to a reset for a defined time (variable cycles, '0' = low active). This is necessary to wait for a stable supply voltage after power up. Basis of this module is a 4 bit counter, which has a default value set to 7 cycle after power up. This counter is programmable by SPI and generates a software reset.

Function: - value for StartUp Reset transfer and initiate Software-Reset (3:0, R) - reading old reset counter register

Command:

Address: 00011111

Data: XXXXXXX XXXXRRRR counter value for reset counter (4 bit)

Program Calibration Register

This register stores the data for the D/A-Comparator. It retains the reference voltage for the high and low limit. Another array of registers stores the frequency of the sine wave generator.

Function:

- high voltage limit for DA-Comparator (15:12, H)
 - low voltage limit for DA-Comparator (11:8, L)
 - frequency of sine wave generator (5:0, F)
 - reading old data from register

Command:

Address: 00000001

Data: HHHHLLLL XXFFFFFF data 16 Bit

High voltage range is 3000mV (b"0000") to 4500mV (b"1111"), default b"1111" Low voltage range is 500mV (b"0000") to 2000mV (b"1111"), default b"0001" Sine wave frequency range is 500kHz (b"000001") to 12MHz (b"11111"), default b"000111"(\approx 2MHz), Setting sine wave frequency \rightarrow b"000000" is not allowed and is hardware-converted to b"000001"

Program Counter Cnt1

Cnt1 counts the cycles for the DA-Comparator to create the reference voltage for the PE5002. It consists of a 10 bit counter. It counts with every clock cycle when enabled from 0 to 1023. In normal mode the counter is static defined from 0 to 1023. In test mode it is possible to manipulate the start value of the counter. In test mode the counter cycles are defined as follows:

Counter cycles = 1023 - SPI programmed value

Function: - programmable only in test mode - set counter start value (9:0, C)

- reading old counter start value

Command:

Address:	00100000	Data:	1
			Test mode on
Address:	0000010	Data:	XXXXXXCC CCCCCCC
			counters data 10 Bit
Address:	00100000	Data:	0
			Test mode off



Program Counter Cnt2

Cnt2 counts the cycles for data transfer to the host PC and the shift cycles in the PE5002. It consists of a 10 bit counter. It counts every clock cycle when enabled from 0 to 1023. The counter is programmable for dedicated data transfer. The formula for shift cycles is:

Shift Cycles = 1023 - SPI programmed value

Function: - setting start count Cnt2 (9:0, C) - read old program data

Command:

Address: 00000011

Data: XXXXXXCC CCCCCCC data 10 Bit

Read states of Main FSM

The Main FSM controls the processes of PE5001, PE5002 and PE5003 in normal operation. In debug mode it is necessary to read data from the state register.

Function: - read data from state register of Main FSM (3:0)

Command:

Address: 00000100

Read states of Write FSM

The Write FSM controls the shift operation in the PE5002 and the data transfer to the host PC. The function provides information about the data in the state register.

Function: - read data from state register of Write FSM (2:0)

Command:

Address: 00000101 Data: XXXXXXXX XXXXXXXX data not necessary

Program Wait-Counter

For a dynamic settling time of the analogue components in PE5002 it is possible to program the Wait –Counter (16 bit). Default value is 640 (with $8MHz = 80\mu s$). It is possible to program the counter from $0\mu s$ to 8ms (CLK = 8MHz). The counter counts from 0 to the programmed data for the settling time.

Function: - Wait Counter for settling time (15:0, W) - reading the old register data

Command:

Address: 00001001 Data: WWWWWWW WWWWWWW data for settling time



Program sine wave buffer gain

This register programs the gain of the sine wave generator. The gain is programmable from 1 (b,1111") to 14 (b,0001"). Default value after power on reset is b"0011".

Function: - data for sine wave generator gain (1-15)(3:0, F)

Command:

```
Address: 00001010 Data: XXXXXXX XXXXFFFF
data for gain
SINCOMP(3:0) - binary
SINGAIN(14:0) - 1 out of 15
```

Program phase shift coefficient

The PE5002 allows to program the phase shift module register. Default value is 128 (Phase 0 degree).

Function:	- setting PCO register (9:0, P)
	- reading the old register data

Command:

Address: 00010000

Data: XXXXXXPP PPPPPPP data 10 bit

Program Gain coefficient

The PE5002 allows to program the input amplifier. Default is 0.

Function: - setting GCO register (9:0, G) - reading the old register data

Command:

```
Address: 00010001
```

Data: XXXXXXGG GGGGGGGG data 10 bit



4.1.2 Main Control

The Main Control FSM (U_PP_MAIN1) implements the following functions:

- Waiting for start of the scan process with a start signal (Snap)
- Reset (low active) all internal/external registers und counters
- Set the control signals, transmit a flag to PE5001
- Waiting for 80 μs (default, SPI registered from 0 to 9ms) to tune the DAC
- data read in for one matrix column
- Wait for a ready signal from data read in counter (Cnt1) and data transfer counter (Cnt2)
- Start the next data transfer (Enable Write Control FSM)
- Wait for the flag from PE5001 to end the scan process
- Start the next Column or wait for the start signal (Snap)





4.1.3 Write Control

The FSM for the data transfer controller (U_PP_WRITE1) will be enabled from the main control FSM. This process is independent from the Main Control FSM and has the following functions:

- Start with enable signal from main control (SyncEn) for normal data transfer
- Start with enable signal from main control (Sync_PC) for start cycle to set PCO
- Set the control signals (SensorFrame and LineFrame)
- Set the new phase-shift-coefficients with RSync
- Start data transfer counter (Cnt2)
- Create a shift signal to transfer data from PE5002 to PE5003 and transfer data to PC
- While shifting data to PC load new phase-coefficients in shift register
- Wait for the ready signal (Cnt2)
- Wait for the next data transfer





4.1.4 Cnt1 and Cnt2

Both counters (U_PP_COUNTER1, U_PP_COUNTER2) have the same architecture. The counters are controlled by the SPI. They have the following functions:

- global reset to reset SPI settings to default values
- reset counter to SPI data
- place start data cycle with SPI
- start counter with Enable (only one cycle necessary)
- counting from SPI data to 1023
- send a ready after finish counting
- produce a shift clock signal during counting
- set an RSync signal
- counter cycle = 1023 SPI data
- single Step in test mode

Cnt1 is only programmable in test mode, the normal function is count from 0 to 1023 for the DAC. Cnt2 is programmable with SPI to optimize the data transfer cycle to host PC.

The counter timing is defined for the DAC-Timing and data transfer convention:



Table 12 -

Name	Function	Timing
ts_cnen – setup Enable	ts_dff	0,8 ns
th_dcnt - hold data count	th_dff	1,2 ns
th_cntrd - hold ready signal	th_dff	1,2 ns

4.1.5 Wait counter

The Wait counter (U_PP_WAIT1) is necessary to define a settling time for the phase shifter in PE5002. It is a 16 bit counter. The function is defined as follows:

- reset counter to 0
- place end data cycle with SPI
- start counter with enable (hold enable during counting)
- send ready after ending counting

This counter is programmable from 0 to 65535. This refers to a time of $8191\mu s$ at 8MHz. Standard is $80\mu s$. The timing definitions are the same as for Cnt1.



4.1.6 Data Registers

The PE5003 has separate registers to store data for several functions:

PCO register	- U_PP_PCO1, 16 Bit register (10 Bit used) - store phase shift information for PE5002 from SPI
GCO register	- U_PP_GCO1, 16 Bit register (10 Bit used) - store gain information for PE5002 from SPI
SCT register	- U_PP_SCT1, 16 Bit register (6 Bit used) - set stimuli clock to tri state information from SPI
CAL register	 set amplification of sinus signal U_PP_CAL1, 16 Bit register (16 Bit used) set sinus frequency information (6 Bit) from SPI
Data buffer	 set upper reference value information (4 Bit) from SPI set under reference value information (4 Bit) from SPI U_PP_BUFF1, 10 Bit register (10 Bit used) synchronize data from PE5002 to PC transfer

4.1.7 Signal Diagram for inner and inter IC communication

Clock- and cycle diagram for inner- and inter- IC communication of PE5003.

	Start Cycl	e by 1024	1	1	I	1
Snap	1//					
CReset_n	L/					
RCntReset_n						
Cflag_out						
CShift						
Cnt1	0 X 1 X	X1022 X 1023 X 0 X	<u>1 2 2 </u>	X 1022 X 1023 X 0		X 798 X 799 X 800 X 801 X
RCLK						
Cnt1Rdy						
SyncEn						
RSync						
RShift				1		
Cnt2Rdy			1	Ш		
SensorF <u>rame</u>						
LineFrame						
D_out				XD1023		0 XD1020 XD1021 XD1022 X D1023

Cycle by 1024



Fundamentals for data transfer are the signals:

Snap	- Starts the sensor matrix scan
SensorFrame	 indicates the first column in "image" transfer to PC
LineFrame	- indicates a line start in "image" transfer to PC
D_out	 10 Bit data bus to PC interface card
PCLK	- pixel clock (name derived from former optical system), same as Clk

The cycle diagram describes the dependency of ready signals Cnt1Rdy and Cnt2Rdy. A new column can only be read, when both signals are high.

The top value of the counter (Cnt2) is static set to 1024, not used rows (>800) are read as PCO from PE5003. Cnt2 is programmable via SPI for user defined transfer steps in 100 cycle steps.

All digital signals are high active. The digital output pins of the system controller, which are driven by the logical signals described here, are slew rate controlled to avoid system interference ensuring high SNR.

The reset signals (CReset_n, RReset_n, RCntReset_n) are designed asynchronously and with low active signals.

4.2 Signal timing definition for host PC communication



The next diagram shows the timing convention for PE5003 to PC communication:



Table 13 -

Name	Function	Timing
th_ck1	th_pinout	2,1 ns
th_ck2	th_neg + th_pinout	0,9 ns + 2,1 ns = 3,0 ns
ts_snap	ts_dff	0,8 ns
th_snap	th_dff	1,2 ns
th_lsf	th_dff + th_pinout	1,2 ns + 2,1 ns = 3,3 ns
th_rs	th_neg + th_pinout + th_pinin	0,9 ns + 2,1 ns + 0,6 ns = 3,6 ns
th_d2	th_dff + th_pinout + th_pinin	1,2 ns + 2,1 ns + 0,6 ns = 3,9 ns
th_d3	th_pinout	2,1 ns

Naming convention:

th_xxx - hold timing ts_xxx - setup timing

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5 Full sensor system overview schematic

Following figure reflects all ICs involved in the sensor matrix communication process.





5.1 Transfer data to PE5003

To transmit data to a host PC, a 10-bit shift register with a multiplexer to load data from sensor data acquisition (10-bit counter) is employed. The cycle of loading and shifting is defined and controlled in the PE5003 and is executed in PE5002 using these shift registers.

The block diagram describes the modules definition.



This regular shift register structure is advanced with a phase coefficient register after the first shift register. This register has a reset with Rreset and will be shifted with rising edge of Rsync.

RRESET	h
RSYNC	
PCO GPC_old X 0 X 1 X 2 X 3 XGPC_XGPC_XGPC_Rew	
PCO_FF DPC_old	GPC_ol
GCO GPC_old X 0 X 1 X 2 X 3 XGPC_XGPC_XGPC_2 XGPC	
GCO_FF GPC_old	GPC_ol



6 Interfaces

Table 14 - Interfaces

гац	Interface	1/0	Function
1	NANDTREE	0	Nand tree test pin
2	Dout9	0	data output for data transmit to PC
3	Dout8	0	data output for data transmit to PC
4	Dout7	0	data output for data transmit to PC
5	Dout6	0	data output for data transmit to PC
6	Dout5	0	data output for data transmit to PC
7	Dout4	0	data output for data transmit to PC
8	Dout3	0	data output for data transmit to PC
9	Dout2	0	data output for data transmit to PC
10	Dout1	0	data output for data transmit to PC
11	Dout0	0	data output for data transmit to PC
12	SNAP	Í	starts one cycle of acquisition
10	LineFreme		barizontal (line) avaptraziantian
13	LineFrame	0	norizontal (line) synchronisation
14	SensorFrame	0	vertical (frame) synchronisation
15	PCLK	0	pixel clock
16	XTout	0	output for crystal oscillator
17	Test	10	Analogue pin for test
18	XTin	Ι	input for crystal oscillator
19	/Reset	Ι	digital core master reset input
20	VrefLcap	0	upper voltage reference level for digital to analogue conversion
21	VrefHcap	0	lower voltage reference level for digital to analogue conversion
22	GNDN0	Ρ	Ground free pins
23	GNDA0	Ρ	Ground analogue core
24	GNDN1	Ρ	Ground free pins
25	GNDA1	Ρ	Ground analogue core
26	CFlag	Ι	input column driver flag chain
27	VDDA0	Ρ	analogue supply voltage
28	CShift	0	shift clock for column driver registers
29	VDDA1	Ρ	analogue supply voltage
30	CReset	0	reset for column driver registers
31	GNDA2	Ĭ	Ground analogue core
20			autout alluma driver flag abain
32			
33	GNDA3	Р	Ground analogue core
34	USC2	0	master stimuli output clock for column
35	VDDA2	Р	analogue supply voltage
36	SDC	0	signal ground for column drivers
37	VDDA3	Р	analogue supply voltage
38	VDDB0	P	supply voltage for pad ring
30	VDDB1	P	supply voltage for pad ring
40	CNDRO	<u> </u>	Ground had ring
40			Ground pad ring
41			Ground pad ning
42	PCo0	0	output for coefficient data to phase- shifting in row chip

43 PCo1 O output for coefficient data to phase-shifting in row chip 44 PCo2 O output for coefficient data to phase-shifting in row chip 45 PCo3 O output for coefficient data to phase-shifting in row chip 46 PCo4 O output for coefficient data to phase-shifting in row chip 47 PCo5 O output for coefficient data to phase-shifting in row chip 48 PCo6 O output for coefficient data to phase-shifting in row chip 49 PCo7 O output for coefficient data to phase-shifting in row chip 50 PCo8 O output for coefficient data to phase-shifting in row chip 51 PCo9 O output for coefficient data to phase-shifting in row chip 52 RReset O reset for AD registers 53 RCNTReset O reset for AD registers 54 REF O used to store A/D value in shift registers 58 RShift O silt clock for serial 60 Din9 1 input for serial data read in (from row chips) 61 Din8 1 input for serial data read	Pad	Interface	I/O	Function
4.3 PCo1 O shifting in row chip 44 PCo2 O output for coefficient data to phase-shifting in row chip 45 PCo3 O output for coefficient data to phase-shifting in row chip 46 PCo4 O output for coefficient data to phase-shifting in row chip 47 PCo5 O output for coefficient data to phase-shifting in row chip 48 PCo6 O output for coefficient data to phase-shifting in row chip 49 PCo7 O output for coefficient data to phase-shifting in row chip 50 PCo8 O output for coefficient data to phase-shifting in row chip 51 PCo9 O output for coefficient data to phase-shifting in row chip 52 RReset O reset for A/D registers 53 RONTReset O reset for A/D registers 54 REF O reference voltage for A/D conversion 55 SDCR O signal ground for row drivers 58 RShift O ingut for serial data read in (from row chips) input for serial data read in (from row chips) 61	40	DO-1	~	output for coefficient data to phase-
44 PCo2 O output for coefficient data to phase-shifting in row chip 45 PCo3 O output for coefficient data to phase-shifting in row chip 46 PCo4 O output for coefficient data to phase-shifting in row chip 47 PCo5 O output for coefficient data to phase-shifting in row chip 48 PCo6 O output for coefficient data to phase-shifting in row chip 49 PCo7 O output for coefficient data to phase-shifting in row chip 50 PCo8 O output for coefficient data to phase-shifting in row chip 51 PCo9 O output for coefficient data to phase-shifting in row chip 52 Reset O reset for AD registers 53 RCNTReset O reset for AD registers 54 REF O reference voltage for AD conversion 55 SDCR O asset stimuli output for serial data read in (from row chips) 61 Din8 1 inter-row-chip interface 59 RCLK O clock for AD registers 62 Din7 1 input for serial data read in (from row chips)	43	PC01	0	shifting in row chip
44 PC02 O shifting in row chip 45 PCo3 O output for coefficient data to phase- shifting in row chip 46 PCo4 O output for coefficient data to phase- shifting in row chip 47 PCo5 O output for coefficient data to phase- shifting in row chip 48 PCo6 O output for coefficient data to phase- shifting in row chip 49 PCo7 O output for coefficient data to phase- shifting in row chip 50 PCo8 O output for coefficient data to phase- shifting in row chip 51 PCo9 O reset for A/D registers 53 RCNTReset O reset for A/D registers 54 REF O reference voltage for A/D conversion 55 SDCR O shift clock for serial inter-row-chip interface 58 RShift O lock for serial inter-row-chip interface 59 RCLK O clock for A/D registers 60 Din3 I input for serial data read in (from row chips) 61 Din6 I input for serial data read in (from row chips) 62	44	PCo2	0	output for coefficient data to phase-
45 PCo3 O shifting in row chip 46 PCo4 O output for coefficient data to phase-shifting in row chip 47 PCo5 O output for coefficient data to phase-shifting in row chip 48 PCo6 O output for coefficient data to phase-shifting in row chip 49 PCo7 O output for coefficient data to phase-shifting in row chip 50 PCo8 O output for coefficient data to phase-shifting in row chip 51 PCo9 O output for coefficient data to phase-shifting in row chip 52 RReset O reset for shift registers 53 RCNTReset O reset for A/D conversion 55 SDCR O signal ground for row drivers 56 OSC1 O master stimuli output clock for row 57 RSync O used to store A/D value in shift registers 58 RCLK O clock for A/D registers 60 Din9 1 input for serial data read in (from row chips) 61 Din8 1 input for serial data read in (from row chips) 62 Din7 <td>44</td> <td>F 002</td> <td>0</td> <td>shifting in row chip</td>	44	F 002	0	shifting in row chip
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66 DSC1 O Image of the second s	55	SDCB	0	signal ground for row drivers
56 OSC1 O Inducts of this output or output of solution output of solutinge	- 55	ODOIN	Ŭ	master stimuli output clock for
57 RSync O used to store A/D value in shift register. 58 RShift O shift clock for serial inter-row-chip interface 59 RCLK O clock for A/D registers 60 Din9 I input for serial data read in (from row chips) 61 Din8 I input for serial data read in (from row chips) 62 Din7 I input for serial data read in (from row chips) 63 Din6 I input for serial data read in (from row chips) 64 Din5 I input for serial data read in (from row chips) 65 Din4 I input for serial data read in (from row chips) 66 Din3 I input for serial data read in (from row chips) 67 Din2 I input for serial data read in (from row chips) 68 Din1 I input for serial data read in (from row chips) 69 Din0 I input for serial data read in (from row chips) 70 SPI_SDO O data output for SPI interface MISO 71 VDDA4 P analogue supply voltage 72 SPI_SDI <td>56</td> <td>OSC1</td> <td>0</td> <td>row</td>	56	OSC1	0	row
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81 VDDR3 P supply voltage for pad ring	80	VDDR2	Р	supply voltage for pad ring
	81	VDDR3	Р	supply voltage for pad ring
82 GNDR2 P Ground pad ring	82	GNDR2	Р	Ground pad ring
83 GNDR3 P Ground pad ring	83	GNDR3	Р	Ground pad ring



7 Dimensions

The PE5003 has following dimensions:

Die size:
Pad size:
Pad middle distance to Die:
Pad middle to pad middle distance:
Pad to Pad distance:
Pad middle (inner ring) to Pad middle (outer ring):
Ring offset (internal to external):
Number of Pads:
Bump material:

4700 μm x 4400 μm 83μm x 83μm 200 μm 300 μm 217μm 300μm 150μm 83 NiAu

MQFP100 packaged devices available on request.



PE5003

Analogue System Controller for Capacitance Sense Solution



8 Contact

Germany

Stuttgart

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