PE5002

100-Channel, 10Bit Capacitance Sense Solution

SERMA PRODUCTIVITY ENGINEERING

Features

- 100 analogue inputs with per channel Lock-in Amplifiers and ADCs
- external reference voltage
- small form factor due to micro bump die attach (wafer scale package possible)
- expandability: cascade several PE5002

Applications

- capacitive sensor signal acquisition
- Touch Screen / Touch Buttons
- Fingerprint Sensor (capacitive arrays)
- laboratory bio-chemical cell growth monitoring
- permittivity based liquid analysis and flow monitoring

General Description

The PE5002 is a 100-channel, 10Bit capacitive sensor signal acquisition circuit. It comprises of all the stages needed for synchronous evaluation (amplification, rectification, A-to-D conversion) of small AC currents in the frequency range 1MHz to 10MHz. Essential building blocks are: current-to-voltage converters, amplifiers, synchronous rectifiers, LP-filters, 10Bit A/D converters and data memory. Each of the circuit stages is implemented once per input line, so parallel operation of all input channels is possible and recommended in terms of power efficiency. The data memory is readable in a serial manner. To cascade the PE5002 and for programming of the internal control registers serial data input is used (daisy chain connection of the several PE5002 circuits).

Functional Description

An AC current from a stimulated capacitive sensor is amplified, transferred into a voltage and rectified. A low pass filter ensures that only the DC component of synchronous demodulation is given to the Analogue-to-Digital converter. The signal is valid on filter output after a settling time defined by the external control scheme. Analogue-to-Digital conversion itself is carried out by supplying a ramp type reference voltage to pin VREF (counting ADC). Needed control signals can be supplied by an external microcontroller or the PE5003. A 10Bit shift register is used to transfer data out of the PE5002. RDIN is the input of the first register and RDOUT the output of the last one. This way it is possible to cascade several PE5002 ICs if more than 100 sensors should be sensed.

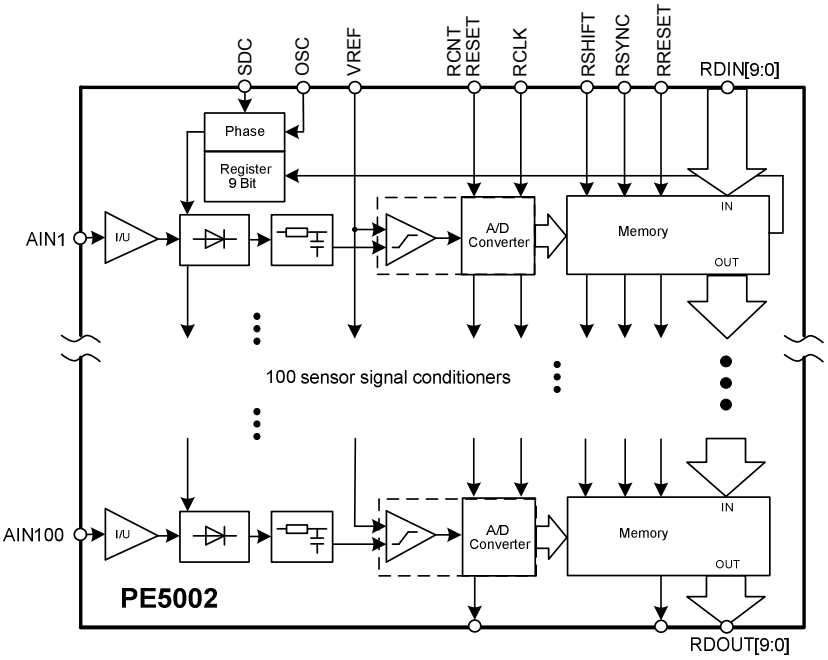

Figure 1: Block diagram

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Electrical Data

All voltages refer to GND = 0V (ground).

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Operating voltage	V_{DD}	-0.3	7	V
Input voltage	V_{IN}	-0.3	V_{DD}+0.3	V
Output voltage	V_{OUT}	-0.3	V_{DD}+0.3	V
Input current	I_{IN}	-10	10	mA
Storage temperature	T_{STG}	-40	125	℃
ESD protection (HBM)	V_{ESD}	2		kV

Stresses exceeding maximum ratings may damage the device. Maximum ratings are stress ratings only. Functional operation above the recommended operating conditions is not implied. Extended exposure to stresses above the recommended operating conditions may affect device reliability.

Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating voltage	V_{DD}	4,75	5	5,25	V
Operating temperature	T_A	-20	27	85	℃
Junction temperature	T_J			<150	℃

Static Properties, I/V Converter, Amplifier, Rectifier and Filter

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Resistance	R_{IN}		40	50	60	kΩ
DC Input Voltage	V_{SDC}		2,3	2,5	2,7	V
Gain V_{out}/V_{IN}	Gain			58		MΩ
OSC DC reference voltage	V_{OSC}		V_{SDC} -0,05		V_{SDC} +0,05	V
Input amplitude OSC	V_{AOSC}		0,1	0,15	0,2	V
Supply current	I_S			60		mA

(V_{DD} = 5V, T=27 ℃)

Static Properties, AD Converter, Data Memory

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Converter input voltage	V_{INREF}		0,5		4,5	V
Converter Offset	V_{OFFSET}			2		mV
Logic Output voltage high	$V_{OUTHIGH}$		4			V
Logic Output voltage low	V_{OUTLOW}				1	V
Output Driver RDOUT	I_O		1			mA
Logic Input voltage high	V_H		3,5			V
Logic Input voltage low	V_L				1,5	V
Input current Pull-Up	I_I				1	µA

(V_{DD} = 5V, T=27 ℃)

Dynamic Properties

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Settling Time	t_{START}				80	µs
AD Converter Bit Time	t_{BIT}		100		135	ns
Serial Clock Cycle	t_{SER}			7,3728		MHz
Counter Delay Time	t_{DZ}	after positive edge			2	ns
Reset Delay Time	t_R	after negative reset edge			2	ns
Data Setup Time	t_{DT}		2			ns
Data Hold Time	t_{DH}		2			ns
Filter Cut Off Frequency	f_{FILT}			100		kHz
Bandwidth I/V Converter	$BW_{I/UW}$		10			MHz
Phase Shifter (per LSB)	t_{PHAS}	f_{OSC} = 1 ... 10MHz	2	3	4	ns
Sensor input voltage	V_{INSEN}	f_{OSC} = 1 ... 10MHz	0,5		2	V
Sensor input Frequency	f_{SEN}		1*		10	MHz

(V_{DD} = 5V, T=27 °C)
*with smaller frequencies it will be more difficult to reach the necessary phases shift

Circuit Description

Lock-in amplifier

PE5002 works with Lock-In amplifiers. Frequencies differing from actual signal frequency or noise are efficiently filtered out this way. *Diagram 1* shows the signal transformation by the Lock-In amplifier. Reference signal OSC is transformed into a square wave and than phase shifted by an adjustable phase shifter to reach a phase difference of 0 degree between the sensor signal and the reference signal (OSC). The central block of a Lock-In amplifier is the rectifier which multiplies both signals.

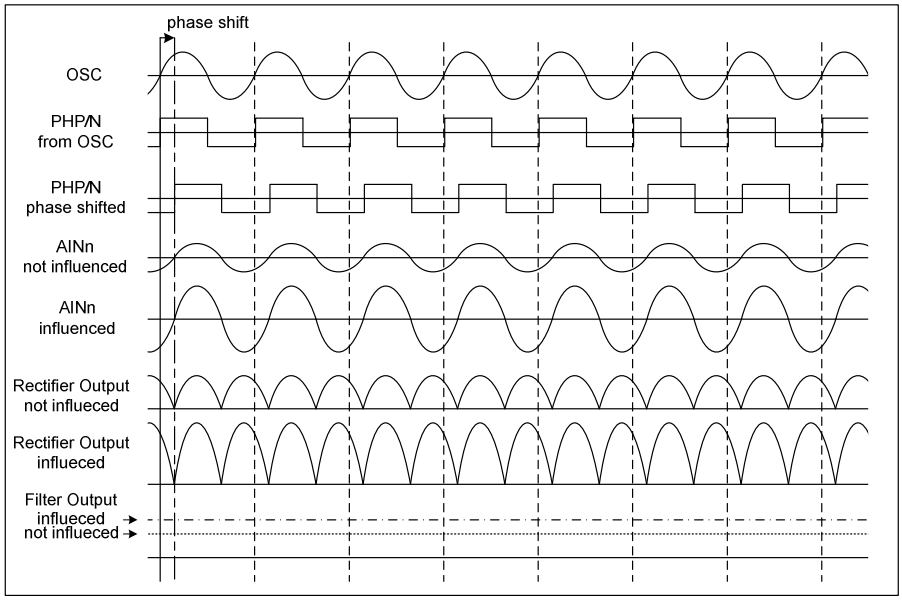


Diagram 1: Principle of signal processing and filtering by a Lock-In amplifier

The stimuli signal for sensor and reference signal (OSC) should have the same source, because if the sensor signal isn't synchronized with reference signal, the average DC-level of the multiplier output is zero (see
Diagram **2**) in this case.

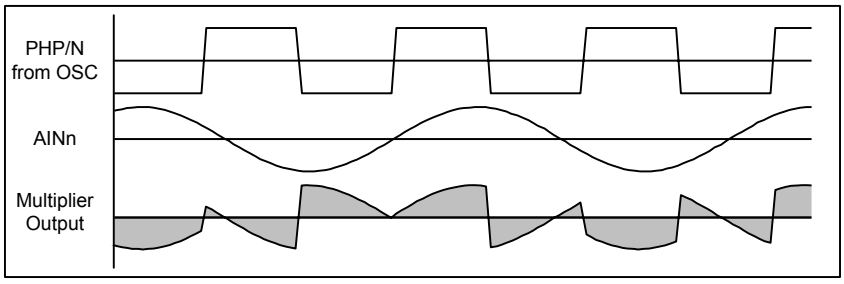


Diagram 2: Principle of signal processing and filtering by a Lock-in amplifier

Phase Shifter

The system specific phase shift of the sensor driver, amplifier and multiplier is corrected with an adjustable phase shifter. Calibration can be done by a 9Bit wide register PCO. The MSB of the register switches the phase by 180 degree, the lower 8Bit are setting the phase shift to one of 256 possible steps. The minimal delay for one LSB defines the maximal phase shift of 768ns (typical). This is equivalent to approx. 180 degree at 650kHz (The phase shifter is implemented as a digital controlled delay line. So the setting for a specific phase shift is frequency dependent!).
The amplitude from the OSC signal shouldn't exceed 200mV, preventing the amplifier from over-modulation.

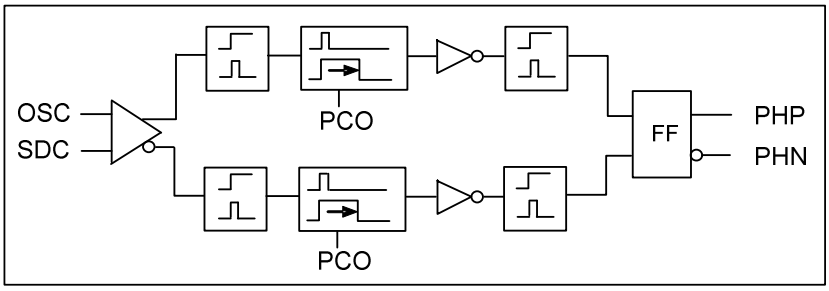


Figure 2: Phase shifter

PCO definition:
Delay: typical for one LSB 3ns (See *Dynamic Properties* on page 4)
Format: RDIN[9:0] <= "XPPPPPPPPP"
| | |----------| - Phase shifter delay PCO[7:0]
| | - Phase inverter PCO[8] (phase switch 180°; with '1')
| - ignored value

Example: RDIN[9:0] <= "0000000001" - 3ns Phase shifting (positive)
RDIN[9:0] <= "0011111111" - 768ns Phase shifting (positive)
RDIN[9:0] <= "0100000001" - 3ns Phase inverse shifting (negative)

Trans-Impedance Amplifier (TIA), Rectifier and Filter

Sensor signal acquisition is carried out by amplification of a capacitance dependent input current by a trans-impedance amplifier and synchronous rectification. The input signal is connected to a trans-impedance amplifier. The trans-impedance itself can be tuned by a 2Bit wide digital control word in GCO (other bits ignored). The capacitive sensor stimulating signal is used for demodulation as well. It is supplied to the OSC pin. The input pin is followed by a digital controllable phase shifter for correcting system dependent phase errors (for synchronous rectification a certain knowledge of system implied phase shift is needed).
Rectification itself is done by a low power analogue multiplier. Due to the demodulation of the input signal, only parts of the signal generated by stimulation are evaluated. Noise and other effects are filtered out by selecting only the DC component after demodulation (Lock-In detection).

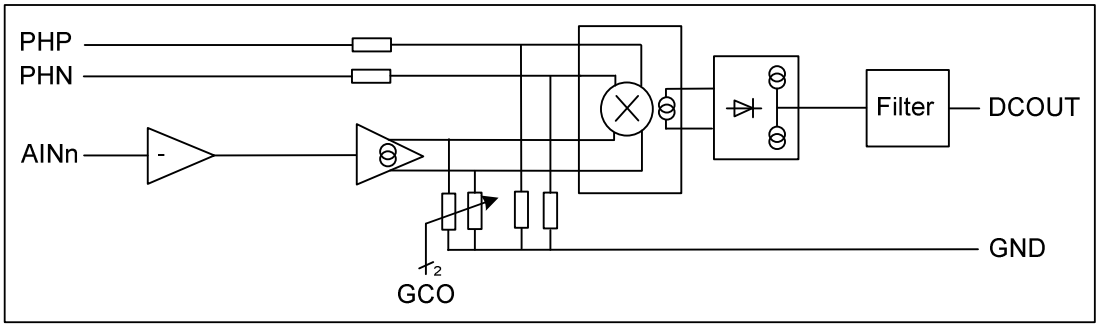
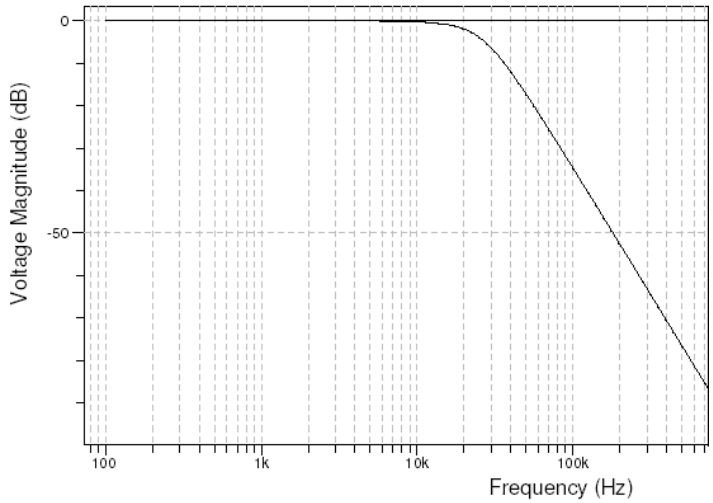


Figure 3: Input signal path

GCO definition:
Format: RDIN[9:0] <= “XXXXXXXXGG”
X = ignored value
GG = GCO[1:0]

GCO[1:0]	Gain / V
“00“	3.03
“01”	3.27
“10”	3.35
“11”	3.73

The Filter is a third order Butterworth filter with the cutoff frequency at about 25kHz. The slope is 60 dB/decade. The typical filter characteristic is depicted in the diagram.



A/D Converter

The A/D converter compares the low pass filtered demodulation product DCOUT (see *Figure* **3**) with VREF supplied by an external reference voltage source. This source has to provide a saw-tooth shaped signal. The lowest and highest edges of the input waveform are defining the ADCs LSB and full scale range. If the output voltage is equal or greater than VREF, a high active STOP signal will store the actual counter value (AD_Register). This register stores the value until the next counter reset. The reset is a low active signal from RCNTRESET. The cycle signal for the counter is the rising edge of RCLK. The counting range is 0 to 1023. Every sensor signal conditioner (AD1 to AD100) has a 10Bit register to save the actual counter value after a STOP condition until the next reset. Those 10Bit values are shifted through the chain and can be read sequentially on RDOUT.

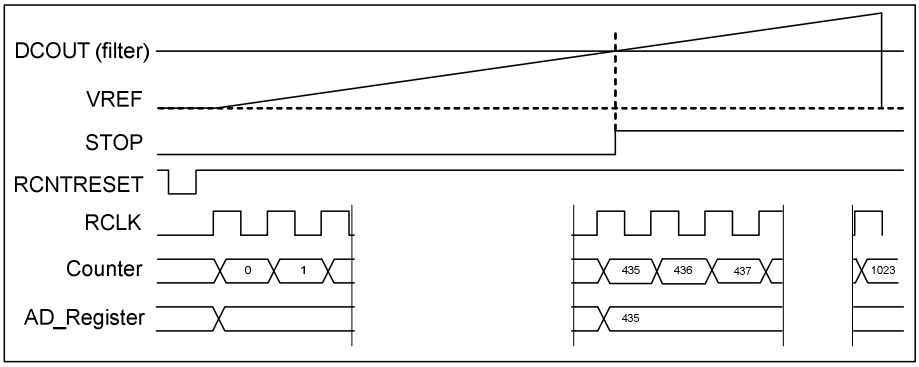


Diagram 3: A/D Converter function

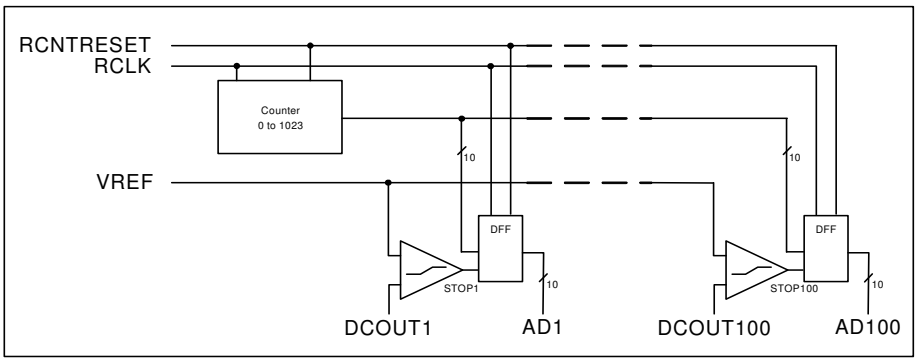


Figure 4: A/D Converter block diagram

Data Memory General Description

The A/D converter results, stored in the registers (signals AD1 … AD100), will be transferred with high active RSYNC and positive edge of RSHIFT in the memory register structure. If RSYNC is low the memory has a shift register structure and every rising edge of RSHIFT shifts 10Bit from input signal RDIN to output signal RDOUT. A low active signal RRESET sets the memory to 0. To configure the phase shifter and amplifier it is possible to use a 9Bit PCO register and a 2Bit GCO register. These registers store their values (from DPCO to PCO or DGCO to GCO) with rising edge of RSYNC.

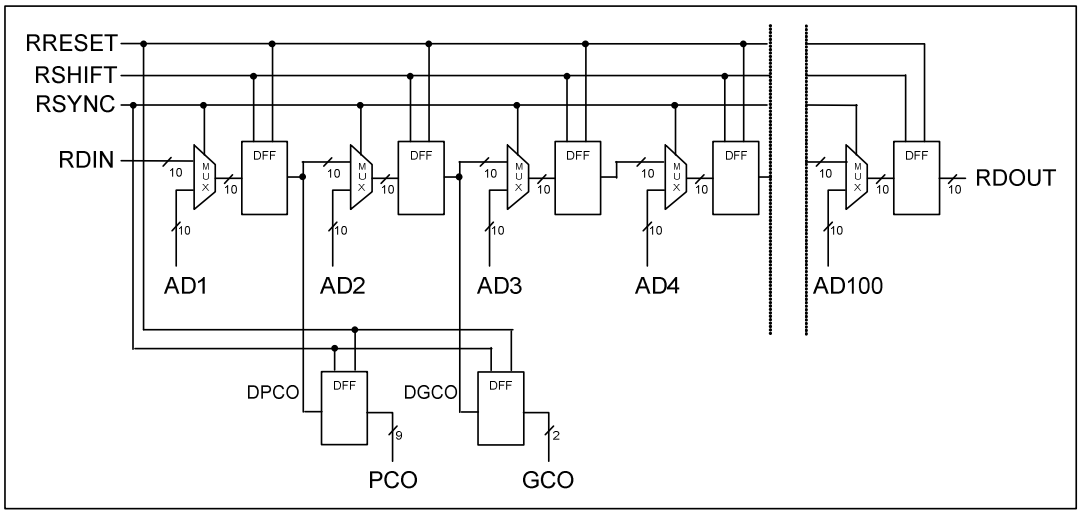


Figure 5: Shift registers structure as data memory

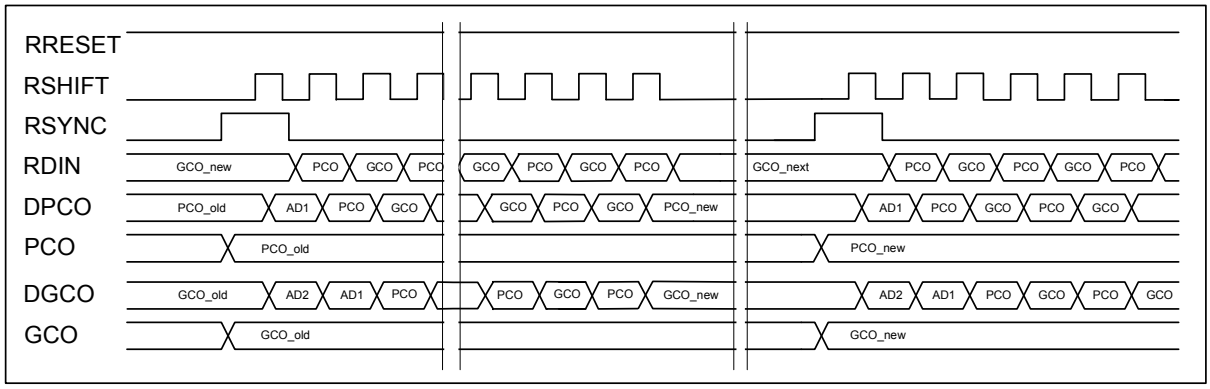


Diagram 4: Relation between RDIN, PCO and GCO cycled by RSHIFT and RSYNC

The PCO and GCO registers are reset able with RRESET. To load PCO and GCO it is necessary to toggle the register data for GCO (even) and PCO (odd) on RDIN with every RSHIFT (see *Diagram 4*) cycle during data transfer (see *Data Transfer to Microcontroller or other PE5002*). This way a cascaded system of PE5002 is loadable with dynamic PCO and GCO values or a dynamic iteration of phase and gain settings is possible during normal function. To initialize the PCO and GCO for the first run it is necessary to toggle two RSHIFT cycles with GCO (even) and PCO (odd) values on RDIN. The values are now active on DPCO and DGCO. A rising edge on RSYNC store the value in PCO and GCO register (see *Communication Flow*).

Counter for Sensor Data Acquisition

For sensor data acquisition (analogue to digital conversion), an external clocked counter is used. This counter is enabled by the corresponding comparator, comparing the supplied reference voltage and signal, generated by analogue input circuitry, representing the value of a sensor element.
Without a stop signal provided by the comparator the counter counts to the maximum value "1111111111".

Data Transfer to Microcontroller or other PE5002

To transmit data to a microcontroller a 10Bit shift register is used (see *Figure 5*). The cycle of loading and shifting has to be defined in the microcontroller and is executed in the PE5002 using these shift registers.
This regular shift register structure is advanced with a phase coefficient register (PCO) after the first shift register and a gain coefficient register (GCO) after the second shift register.

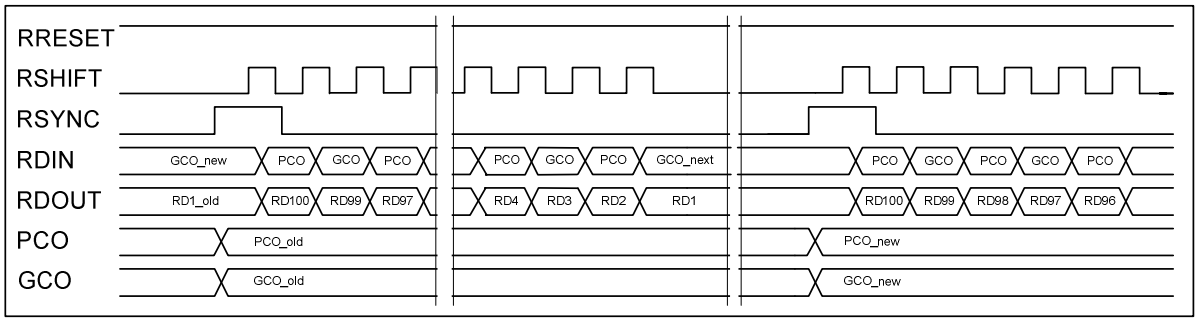


Diagram 5: Cycle diagram for relation between RDIN and RDOUT

Timing Convention for Data Transfer from PE5002 to PE5002 or to MCU

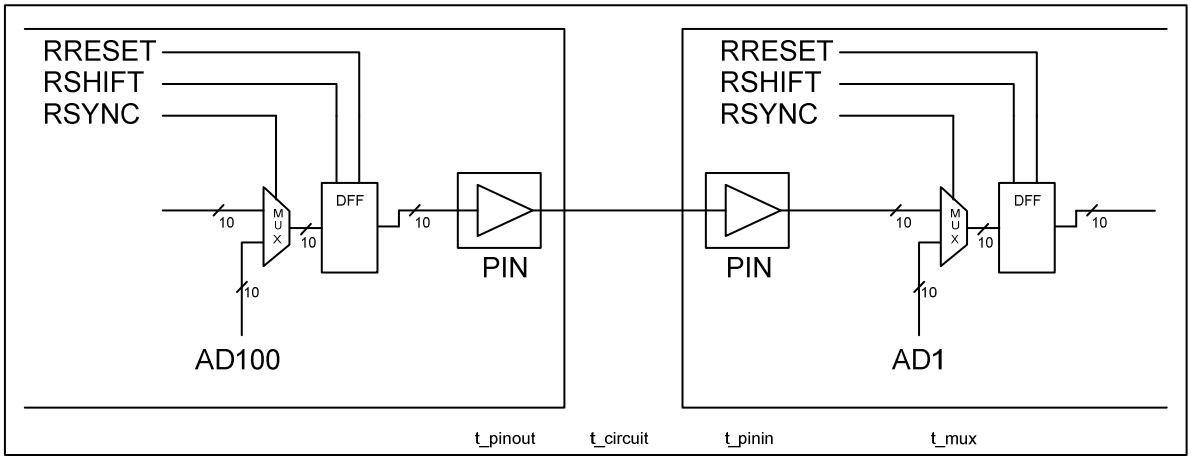


Figure 6: Timing convention for Data transfer

The timing function with synchronised data transfer is defined as follows:

1/Clk > t_pinout + t_circuit + t_pinin + t_mux

t_circuit < 1/Clk – t_pinout – t_pinin – t_mux

t_circuit < 121,6 ns

Standard Cell CMOS timing diagram	
t_pinout	2,1 ns
t_pinin	0,6 ns
t_mux	0,7 ns
Clk	8 MHz
1/Clk	125 ns

Interfaces

Pad	Name	IO-Typ	Function
1	AIN91	I	Matrix row 91
...	...		...
10	AIN100	I	Matrix row 100
11			nc
...			...
14			nc
15	RDO0	O	Serial data output 0
16	RDO1	O	Serial data output 1
17	RDO2	O	Serial data output 2
18	RDO3	O	Serial data output 3
19	RDO4	O	Serial data output 4
20	RDO5	O	Serial data output 5
21	AIN81	I	Matrix row 81
...	...		...
30	AIN90	I	Matrix row 90
31			nc
...			...
34			nc
35	RDO6	O	Serial data output 6
36	RDO7	O	Serial data output 7
37	RDO8	O	Serial data output 8
38	RDO9	O	Serial data output 9
39	RRESET	O	Reset shift register (*)
40	RCNTRESET	O	Reset ADC counter (*)
41	AIN71	I	Matrix row 71
...	...		...
50	AIN80	I	Matrix row 80
51			Not existent, positioning marker
52			nc
...			...
60			nc
61	AIN61	I	Matrix row 61
...	...		...
70	AIN70	I	Matrix row 70
71	VCCA	P	Supply voltage, 100nF
...	...	...	...
80	VCCA	P	Supply voltage, 100nF
81	AIN51	I	Matrix row 51
...	...		...
90	AIN60	I	Matrix row 60
91	VCC	P	Supply voltage, 100nF
...	...	...	...
98	VCC	P	Supply voltage, 100nF
99	TESTA	I/O	Test Pin 1
100	TEST1	I/O	Test Pin 2
101	AIN41	I	Matrix row 41

Pad	Name	IO-	Function
...	...		...
110	AIN50	I	Matrix row 50
111	GND	P	Ground
...	...	...	...
118	GND	P	Ground
119	TEST	I/O	Test Pin 3
120	TEST3	I/O	Test Pin 4
121	AIN31	I	Matrix row 31
...	...		...
130	AIN40	I	Matrix row 40
131	GND	P	Ground
...	...	...	...
140	GND	P	Ground
141	AIN21	I	Matrix row 21
...	...		...
150	AIN30	I	Matrix row 30
151			nc
...			...
159			nc
160	RCLK	I	ADC counter clock
161	AIN11	I	Matrix row 11
...	...		...
170	AIN20	I	Matrix row 20
171	RDI1	I	Serial data input 1
172	RDI3	I	Serial data input 3
173	RDI5	I	Serial data input 5
174	RDI7	I	Serial data input 7
175	RDI9	I	Serial data input 9
176	RCNTRESET	I	Reset ADC counter (*)
177	VREF	I	ADC reference (**)
178	SDC	I	Signal ground for row, 10nF extern (**)
179	OSC	I	Sinus oscillator input
180	RSHIFT	I	Shift register clock
181	AIN1	I	Matrix row 1
...	...		...
190	AIN10	I	Matrix row 10
191	RDI0	I	Serial data input 0
192	RDI2	I	Serial data input 2
193	RDI4	I	Serial data input 4
194	RDI6	I	Serial data input 6
195	RDI8	I	Serial data input 8
196	RRESET	I	Reset shift register (*)
197	VREF	I	ADC reference (**)
198	SDC	I	Signal ground for row, 10nF extern (**)
199	OSC	I	Sinus oscillator Input
200	RSYNC	I	Serial / parallel switch

(*) CNTRESET and RRESET signals, internal connection from input to output, feature for daisy chain of PE5002
(**) doubled analogue input pins, better connectivity for flip chip assembly

Dimensions

The PE5002 has following dimensions:

Die size:	4675 µm x 6700 µm
Pad size:	76µm x 76µm
Pad distance to X direction Die:	112 µm
Pad distance to Y direction Die:	162µm
Pad to pad distance X direction:	174 µm
Pad to pad distance Y direction:	8*394µm, 1*439µm

Distance between 110 / 10 pad row X direction: 1824µm

Layout X direction: 10 pad rows evenly distributed
2*112µm (border) + 20*76µm (pad) + 18*174µm (distance) + 1824µm (distance) = 6700µm

Layout Y direction: 9 Pad- rows evenly distributed, the 10th row with 439µm distance
2*162µm (border) + 10*76µm (pad) + 8*394µm (distance) + 1*439µm(distance = 4675µm

Bump material: NiAu

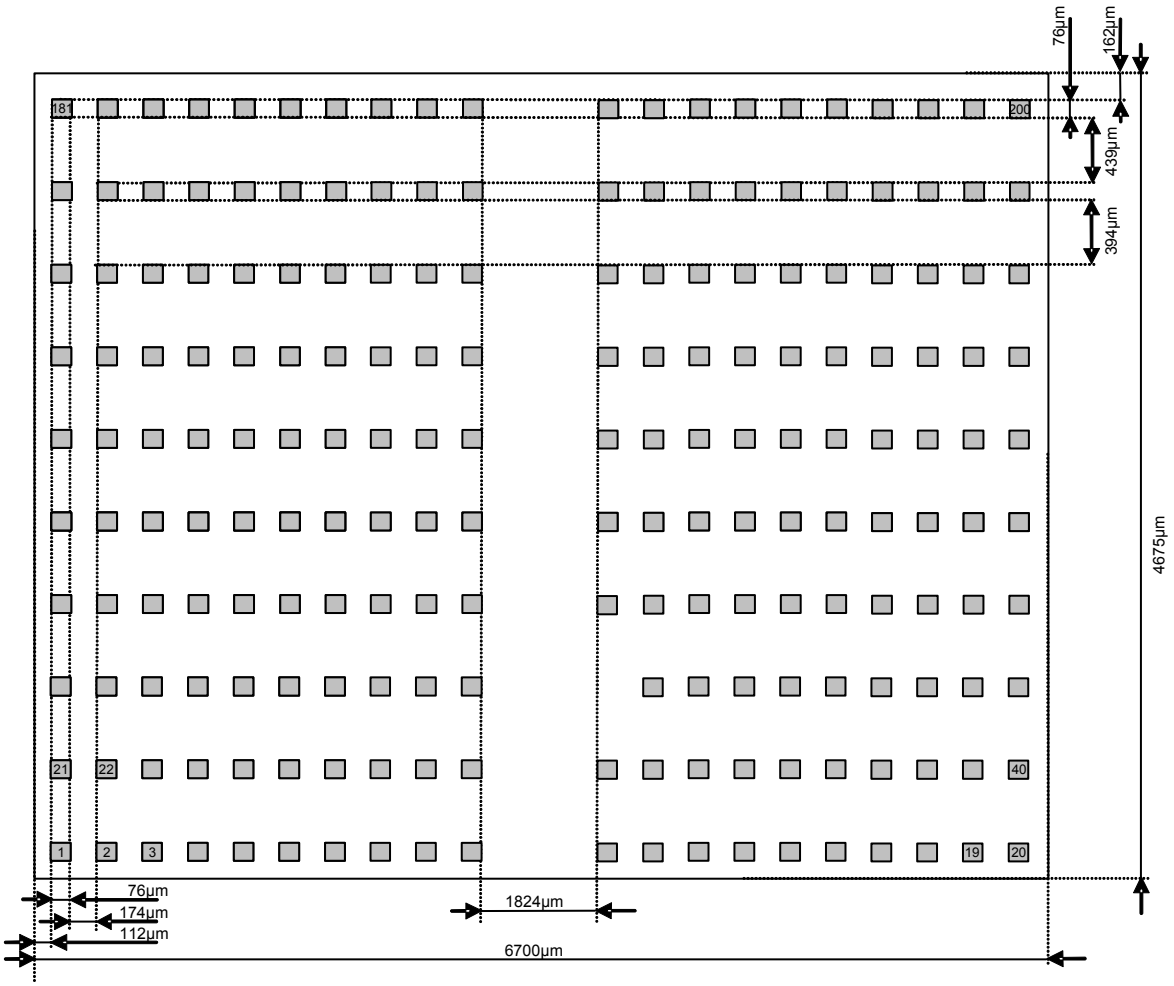


Figure 7: Top view of PE5002

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This project was supported by Award No. 2005-IJ-CX-K067 awarded by the National Institute of Justice, Office of Justice Programs, US Department of Justice. The opinions, findings, and conclusions or recommendations expressed in this publication/program/exhibition are those of the author(s) and do not necessarily reflect the views of the Department of Justice.