PE4301

CCM PFC controller
Power Factor Correction

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Features

- Wide Range Input
- Low Total Harmonic Distortion (THD)
- Low Start Up Current (<5µA)
- Low Operating Current (<550µA)
- Disable Function (<100µA)
- Under-Voltage Lockout with >8V Hysteresis
- Over voltage protection, Peak current protection and
- Open loop protection with separate integrated reference
- Low Peak current protection threshold
- Operating Frequency from 32 kHz to 350kHz, dependent on load
- High Efficiency at high and low Output Power
- Internal Clamping Resistor at Driver
- Soft start
- Fast Driver Switch 'off'

- **Applications**
- Active power factor correction
- Switch mode power supplies

General Description

The PE4301 is a wide input range controller IC for active power factor correction converters.
The IC operates in the CCM with average current control. The switching frequency depends upon the load. At high output the load frequency is low and with low load the frequency increases. The compensation for voltage loop and soft start is external. The PE4301 provides many protection functions, such as over voltage protection for output voltage and for supply voltage, open loop protection, supply under voltage lock-out, output under voltage protection and peak current limit protection. These protection functions work with separate internal references for even higher security. If an error in the regulation reference occurs, the protection function becomes operational. The soft start function limits start up current and stress on the boost diode.
When the disable function is activated, the current consumption drops below 150µA.

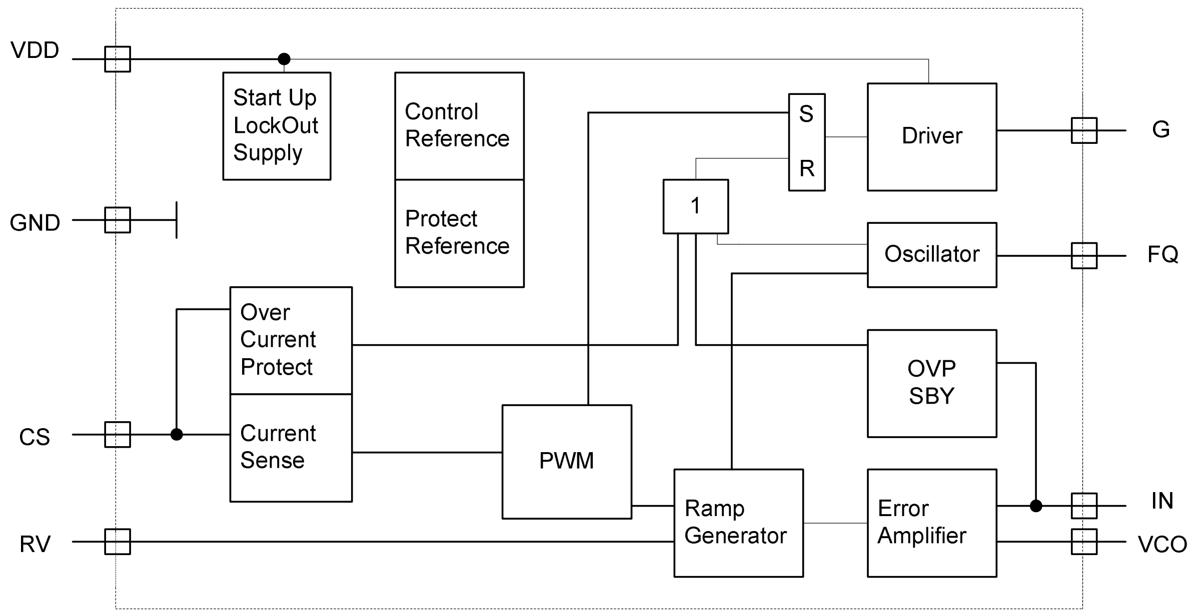

Figure 1 - Block diagram

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Initial Version V1.0	05/2008		
V1.1	06/2010	Storage Temp.	3
V1.2	09/2010	Input Voltage (Pin8)	3

2 Ratings

2.1 Absolute Maximum Ratings

Table 1 – Maximum Ratings

Parameter	Symbol	Min	Type	Max	Unit	Notes
Operating Temp	$T_{junction}$	0		125	℃	
Storage Temp	T_{Sto}	-55		150	℃	
Supply voltage	V_{DD}	-0.3		30	V	
Input voltage (Pin8)	V_{CS}	-40		+40	V	
Input voltage (all other)	V_{IN}	-0.3		V_{DD}+0.7	V	
Output voltage	V_{OUT}	-0.3		V_{DD}+0.7	V	
Input current	I_{IN}			10	mA	

Stresses exceeding maximum ratings may damage the device. Maximum ratings are stress ratings only. Functional operation above the recommended operating conditions is not implied. Extended exposure to stresses above the recommended operating conditions may affect device reliability.

2.2 Operating Conditions

Table 2 – Operating Conditions

Parameter	Symbol	Min	Type	Max	Unit	Notes
Operating Temp	$T_{junction}$	0	27	125	℃	
Supply voltage	V_{DD}	8	14	25	V	

2.3 Detailed Electrical Ratings

Table 3 - Static Operating Conditions ($T_{junction}$ = 0 …125 ℃; StartUp and Supply):

Parameter	Symbol	Min	Type	Max	Unit	Notes
Start Up Voltage	V_{ST}	16		23	V	
Lock Out Voltage	V_{LO}	6,5		7,5	V	
StartUp/LockOut Hysteresis	V_{STLOHY}	11		16	V	
Supply current	I_{DD}			5	µA	before StartUp, V_{DD} <
		180		550	µA	aktiv Operation, without driver load
		30		100	µA	aktiv and disable V_{IN}=0.3V
VDD over voltage protection	V_{DDOVP}	23		31	V	
Voltage at FQ Pin	V_{FQ}	0.950	1.005	1.045	V	R_{FQ} = 100KΩ, T=0 to 50 ºC, will be adjusted
		0.965	1.005	1.045	V	R_{FQ} = 100KΩ, T=0 to 80 ºC, will be adjusted

Table 4 - Static Operating Conditions ($T_{junction}$ = 0 …125 °C; VDD=14V, Protection Function):

Parameter	Symbol	Min	Type	Max	Unit	Notes
Open Loop Protection / Enable (OLP), V_{IN} Threshold	V_{INOLP}	0.29	0,33	0.36	V	
Open Loop Protection / Enable (OLP), V_{IN} Hysteresis	HY_{NOLP}	70	80	100	mV	
Output Over Voltage Protection, V_{IN} Threshold	V_{INOVP}	2.64	2,70	2.75	V	
Output Over Voltage Protection, V_{IN} Hysteresis	HY_{INOVP}	70	80	100	mV	
Peak Current Protection V_{CS} Threshold	V_{CSPCP}	-1.0	-0.9	- 0.7	V	
CS Input current	I_{CS}	-20	-9	-4	µA	V_{CS} = -0.4V

Table 5 - Static Electrical Characteristics: Current Loop (VDD = 14V $T_{junction}$= 0 to 125 ºC)

Parameter	Symbol	Min	Type	Max	Unit	Notes
CS Gain	G_{CS}	-7.9	-8	-8.1		
Input Offset Voltage	V_{OFFCS}		1	3	mV	
Input resistor	R_{CS}	60	64	113	kΩ	

Table 6 - Static Electrical Characteristics: Voltage Loop(VDD = 14V $T_{junction}$= 0 to 125 ºC)

Parameter	Symbol	Min	Type	Max	Unit	Notes
OTA Referenz Voltage	V_{INREF}	2.50	2.58	2.65	V	
OTA Gain	Gm_{OTA}	90	140	190	µS	
OTA linear Range	I_{OTA}	-12		12	µA	$V_{IN} = V_{INREF} \pm 0.13V$, V_{VCO} = 2.5V
Output high voltage	V_{OTAOH}	4.4			V	V_{IN} = 0.5V
Output low voltage	V_{OTAOL}			0.4	V	V_{IN} = 4.5V
Input current V_{IN}	I_{IN}	-0.1		0.1	µA	
Max Output current ±	I_{OTAmax}	|16|		|100|	µA	

Table 7 - Static Electrical Characteristics: Driver (VDD = 18V $T_{junction}$= 0 to 125 ºC)

Parameter	Symbol	Min	Type	Max	Unit	Notes
Output Voltage High	V_{GH}	7,5	8.5	10	V	I_{OH} = -50mA
Output Voltage Low	V_{GL}	1,2	1.5	2.2	V	I_{OL} = 200mA
Maximum Output Voltage	V_{GMAX}	8,0	8,5	9,5	V	
Output Voltage before StartUp and after LockOut	V_{GST}			1	V	
Clamping Resistor	R_G	15	21	27	KΩ	

Table 8 - Dynamical Operating Conditions (VDD = 14V, $T_{junction}$= 0 to 125 ºC):

Parameter	Symbol	Min	Type	Max	Unit	Notes
Driver rise time	t_{Gr}	2		50	ns	C_G = 1nF, V_G rise from 2V to 7V
Driver fall time	t_{Gf}	2		20	ns	C_G = 1nF, V_G fall from 7V to 2V
Peak Current Protection delay	t_{CSPCP}	150		600	ns	
Oscillator Frequency	F_{OSZ}	50		70	kHz	R_{FQ}=100KΩ, V_{VCO}=2.5V
Min Oscillator Frequency	F_{OSZmin}	32		40	kHz	R_{FQ}=100KΩ, V_{VCO}=4.5V
Max Oscillator Frequency	F_{OSZmax}	230		350	kHz	R_{FQ}=100KΩ, V_{VCO}=0.5V
Max Duty Cycle	D_{MAX}	92		99	%	V_{VIN}=2.0V, V_{CS}=0V
Min Duty Cycle	D_{MIN}			0	%	V_{VIN}=2.0V, V_{CS}=-0.6V
Duty Cycle at V_{VIN}=2.0V, V_{CS}=-0.2V		84		91	%	without resistor at RV
		85		90	%	R_{RV} = 100kΩ
Min 'off' time	t_{OFF}	300		1000	ns	V_{CS}=0V

3 Functional Description

3.1 General

The PE4301 is an 8-pin analog controller IC for power factor correction converters. It is suitable for wide range line input applications from 85 to 265 VAC. The IC supports converter in boost topology and it operates in continuous conduction mode (CCM) with peak current control. The IC operates with two loops, an inner current loop and an outer voltage loop. The inner current loop is fast, reliable and does not require sensing of the input voltage in order to create a current reference. This inner current loop sustains the sinusoidal profile of the average input current based on the dependency of PWM duty cycle on the line input voltage to determine the corresponding input current. The outer voltage loop controls the DC output voltage. This voltage is fed into the voltage error amplifier to control the amplitude of the average input current. The two loops combine to control the amplitude, phase and shape of the input current, with respect to the input voltage, giving near-unity power factor. For a better regulation range, the operating frequency is modulated with the voltage loop. If the load is low and the input voltage high, the frequency increases; if the load is high and the input voltage is low, the frequency decreases. The IC is equipped with various protection features to ensure safe operating condition for the system and the device.

3.2 Typical Application Circuit

Figure 2 gives an impression about the external components required for a typical application environment.

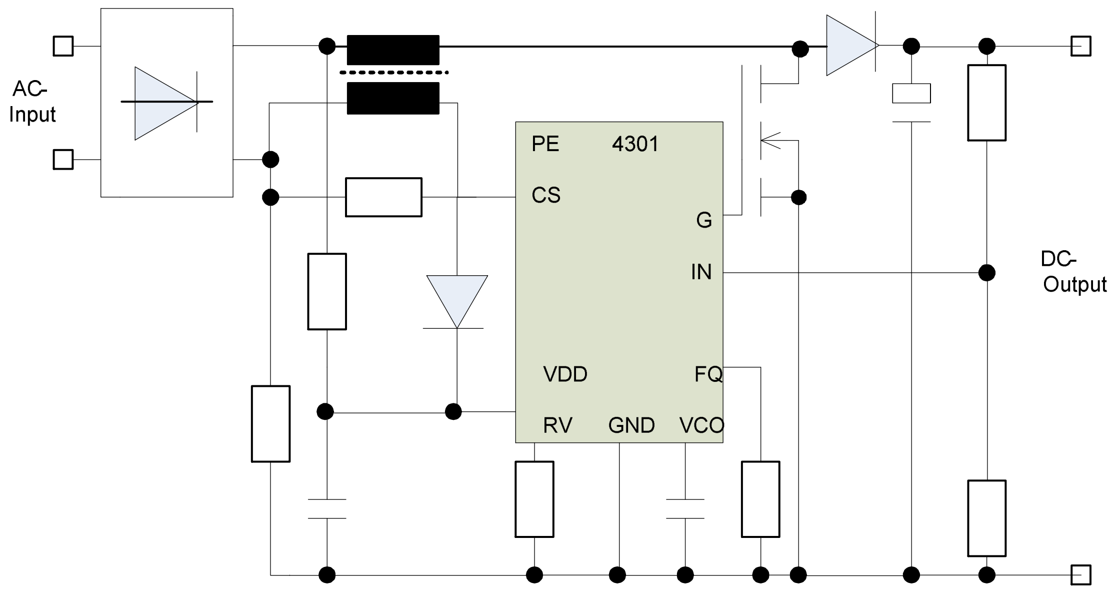


Figure 2 - External component schematic

3.3 Power Supply Startup behaviour

The start-up and under voltage lockout circuit monitors VDD. If VDD rises over the start-up voltage, the system starts normal operation. If VDD falls below the lockout voltage the system turns off. The IC can be turned off and forced into standby mode by pulling down the voltage at pin IN below the OLP threshold voltage level.

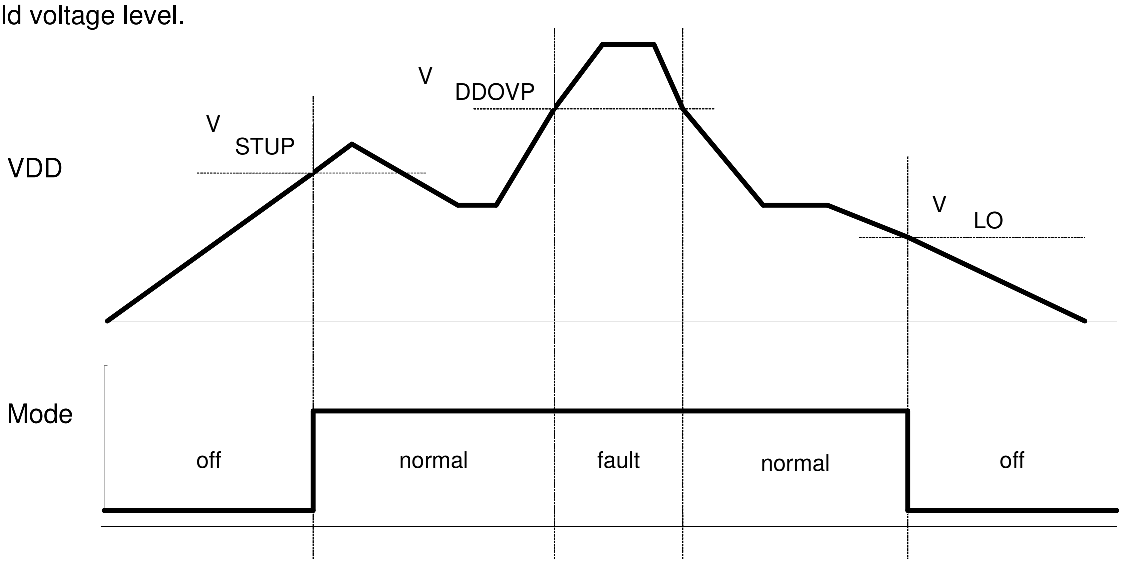


Figure 3 - Startup and shut down sequence

3.4 Gate driver behaviour

The gate driver is a totem pole driver, designed for direct drive of external power MOSFET`s. The high output is clamped at V_{GMAX}.

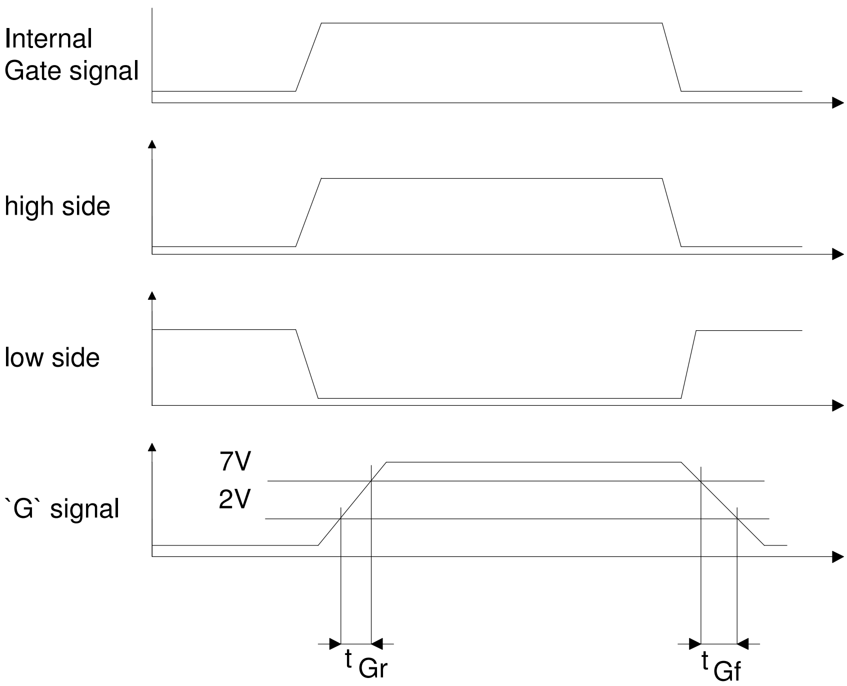


Figure 4 - t_{Gr} and t_{Gf} represent the rise and fall time for the gate driver output assuming a capacitive load of 1nF

3.5 Fault Protection

The fault mode will be activated, when any of the protection circuits crosses the threshold. In fault mode the driver turns “off” or/and the duty cycle is reduced. The IC automatically resumes operation, when the protection circuits return above the threshold level.

1. Output over voltage protection (OOVP) is activated when the voltage at Pin IN rises above V_{INOVP} (figure 5).

2. Open loop protection (OLP) is activated when the voltage at pin IN falls below V_{INOLP}, or there is an insufficient input voltage for normal operation. This function can be used for external disable of the IC (figure 6).

3. Peak current limit protection (PCLP) is activated, when the voltage at pin CS drops below V_{CSPCP}. Short impulses, <300ns, are suppressed with the leading edge time. The driver turns off very fast (t_{sc}) (figure 7).

4. VDD over voltage protection (VDDOVP) is activated, when the voltage at Pin VDD increases to V_{VDDOVP}.

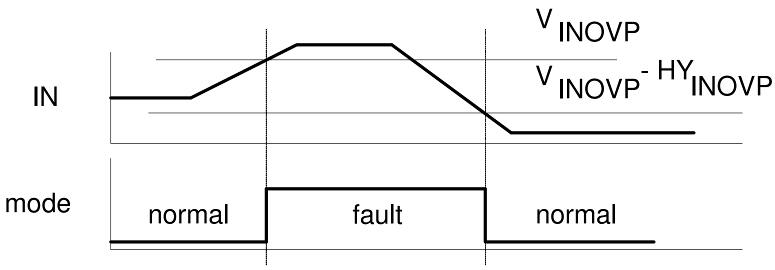


Figure 5 - Output over voltage Protection

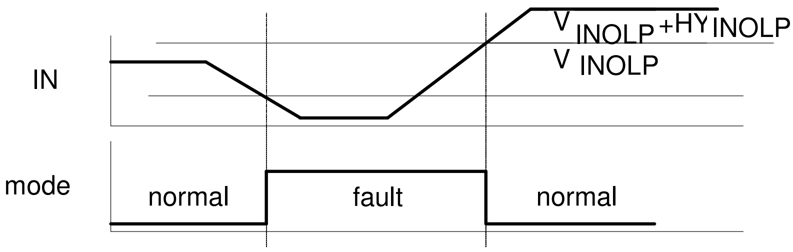


Figure 6 - Output Open Loop Protection

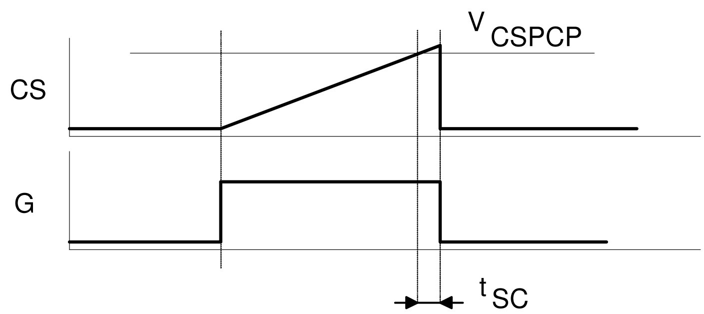


Figure 7 - Peak current limit protection

3.6 Soft start

The soft start function can be realised with the capacitor at pin VCO. The output current of the voltage loop OTA and the capacitor generates a slowly ramp up for the voltage at pin VCO. With this ramp the duty cycle goes from minimal to nominal value.
Soft start time is determined by the following equation:

$$t_{SS} = \frac{C_{VCO} \cdot V_{VCO\,(eff)}}{I_{OTAmax}}$$

3.7 Current control

The current loop block is monitoring the voltage at pin CS, resulted from the inductor current flow trough the current sense resistor. The amplifier with a gain of -8, generates the current comparator signal for the PWM block.

3.8 Average voltage control

The voltage loop block senses the feedback voltage at pin IN. The compensation for the voltage loop is connected to pin VCO. The error voltage at pin VCO is the base for the voltage comparator signal.

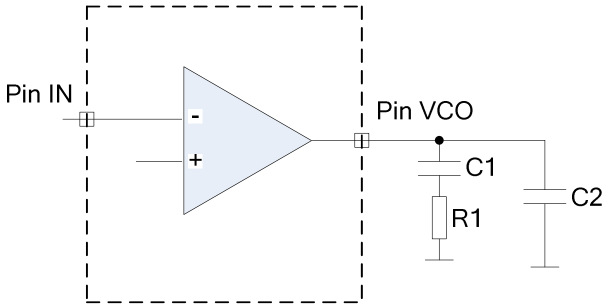


Figure 8 - compensation schematic

Transfer function:

Zero:

$$f_{zo} = \frac{1}{(2 \cdot \pi \cdot R1 \cdot C1)}$$

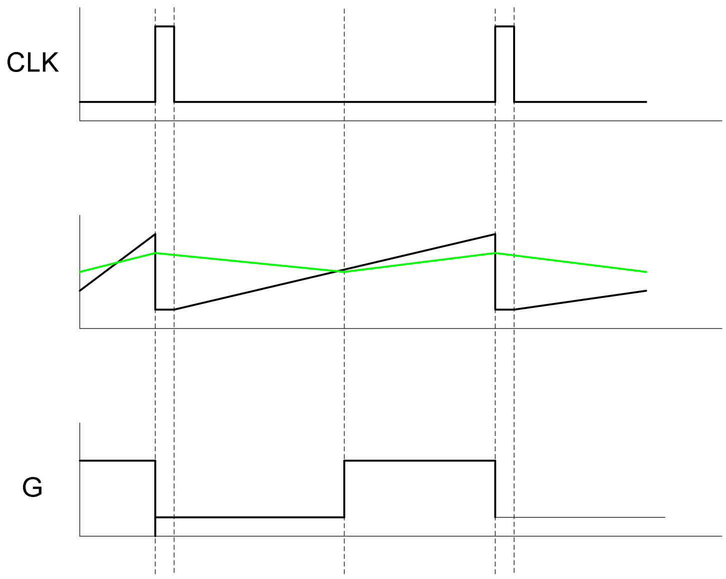
Pole:

$$f_{po} = \frac{1}{2 \cdot \pi \cdot R1 \cdot \frac{C1 \cdot C2}{C1 + C2}}$$

3.9 Ramp generator and PWM

The PWM block includes two ramp generators - one for the duty cycle and one for the switching frequency. If the duty cycle ramp crosses the current comparator signal from the current control, the driver turns off. If the switching frequency ramp crosses the oscillator comparator signal from the oscillator, the driver turns on.

The slew rate of the frequency ramp is defined by the resistor at pin FQ. The slew rate of the duty cycle ramp is calculated from the voltage comparator signal and an internal resistor. For higher accuracy calculation, it is possible to use a resistor at pin RV to adjust the slew rate of the duty cycle ramp. The oscillator comparator signal is calculated from the voltage comparator signal.



Equation for Cso and RampDC:

$$V_{CSo} = G_{CS} * V_{CS}$$

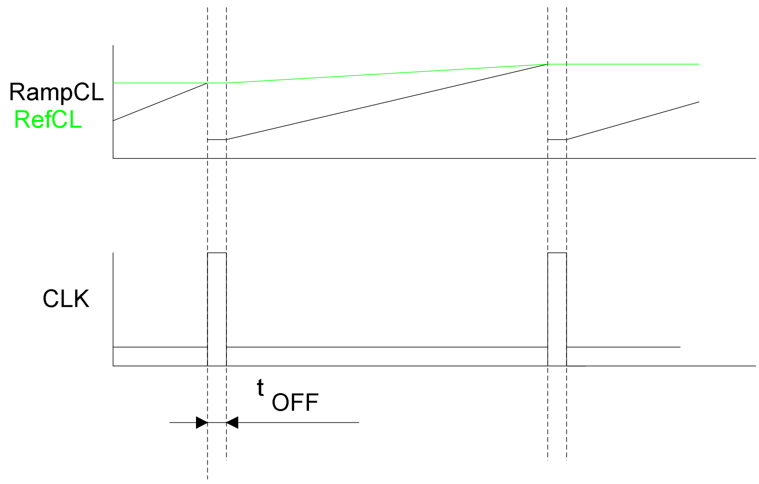
Without RV

$$V_{Ramp\,DC} = f\left(\frac{1}{R_{FQ}} + \frac{V_{VCO}}{100}\right)$$

With RV

$$V_{Ramp\,DC} = f\left(\frac{1}{R_{FQ}} + \frac{V_{VCO}}{R_{RV}}\right)$$

Figure 9 - duty cycle modulation



Equation for RefCL and RampCL:

$$V_{RefCL} = 0.3 + f\left(V_{VCO}\right)$$

$$V_{RampCL} = f\left(\frac{1}{R_{FQ}}\right)$$

Figure 10 - clock modulation

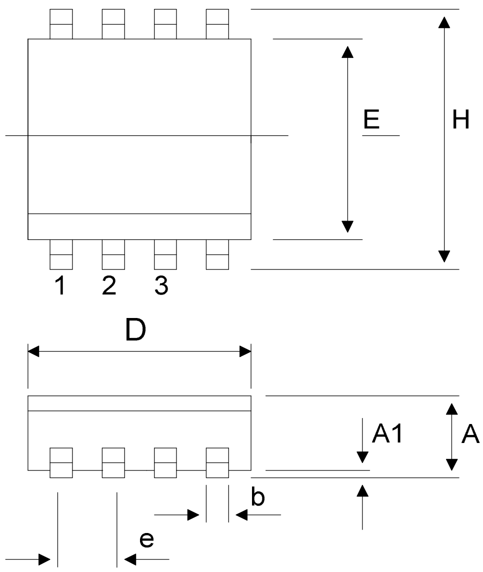
4 Interfaces

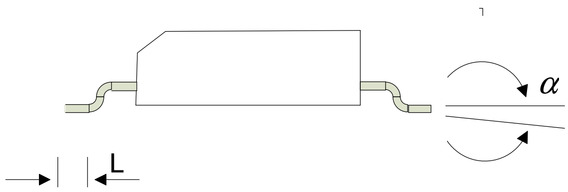
Table 10 - Interfaces

Pin	Pad	Interface	I/O	Function
1	1	VCO	I/O	Voltage Compensation
2	2	IN	I	Regulation Input
3	3	FQ	I/O	Frequency Adjustment
4	4	RV	I/O	Ramp Adjustment
5	5	VDD	I	Power Supply
6	6	G	O	Driver Output
7	7	GND	I	Power Ground
8	8	CS	I	Current Sense

5 Package

The PE4301 comes in an SOIC8 package.





Dim.		D	E	H	A	A1	e	B	L	Copl	α
mm	min max.	4.80 5.00	3.80 4.00	5.80 6.20	1.35 1.75	0.10 0.25	1.27	0.33 0.51	0.40 1.27	 0.10	0° 8°
inch	min max.	0.189 0.197	0.150 0.157	0.228 0.244	0.053 0.069	0.004 0.010	0.050	0.013 0.020	0.016 0.050	 0.04	0° 8°

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The project is funded in parts by the European fund for regional development (EFRE) and the state of Saxony.